

USB オーディオ-I²S デジタル・オーディオ・ブリッジ

CP2615 データシート

CP2615 デバイスは、USB ベースのオーディオ・アプリケーションの迅速な開発を可能にする目的で設計されています。

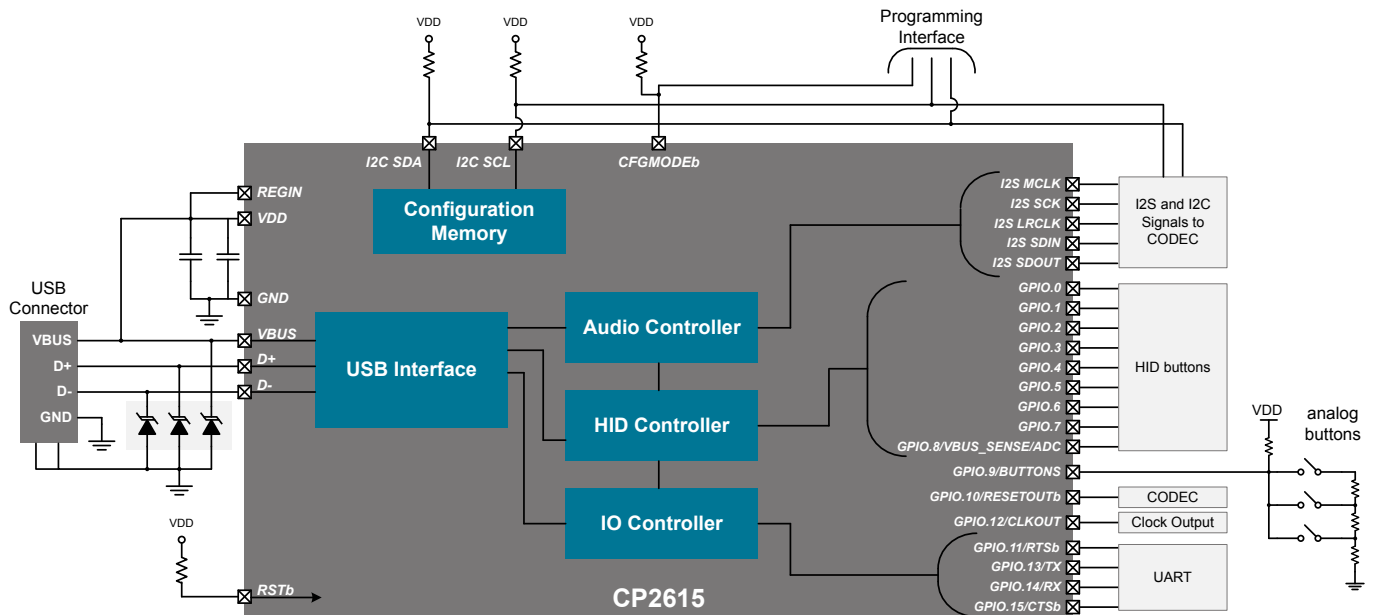
CP2615 は、コードを開発する必要がなく、USB から I²S へのオーディオ・データ転送プロセスを簡素化します。これにより、USB スピーカー、USB ヘッドフォン、USB オルゴール、VoIP システムなどの USB オーディオ・アクセサリの製品化までの時間を短縮することができます。CP2615 には、USB 2.0 フルスピード機能コントローラ、USB トランシーバ、発振器、I²S (オーディオ) インターフェイス、I²C (コントロール) インターフェイス、および UART インターフェイスが含まれています。コンパクトな 5 x 5 mm の QFN-32 パッケージで、スペースに制約のあるポータブル・オーディオ・アプリケーションに最適です。

CP2615 デバイスは、以下を含む広範な USB オーディオ・アプリケーションに最適です。

- ・ USB スピーカー
- ・ MP3 アクセサリ
- ・ ナビゲーション・システム
- ・ USB ヘッドホン/ヘッドセット
- ・ POS 端末
- ・ オルゴール

主な機能

- ・ USB オーディオ・クラス 1.0
- ・ オーディオとメディアに適した USB HID コンシューマ制御に対応
- ・ USB-UART ブリッジ機能を搭載
- ・ 48 kHz、16 ビット/24 ビット・ステレオ・デジタル・オーディオをサポート
- ・ 統合された USB トランシーバ、外部抵抗不要
- ・ 統合されたクロック、外部水晶不要
- ・ オンチップ電圧レギュレータ : 3.45 V 出力
- ・ セルフパワーまたはバスパワー
- ・ ファームウェア開発不要



第 1 章 機能リストと注文情報

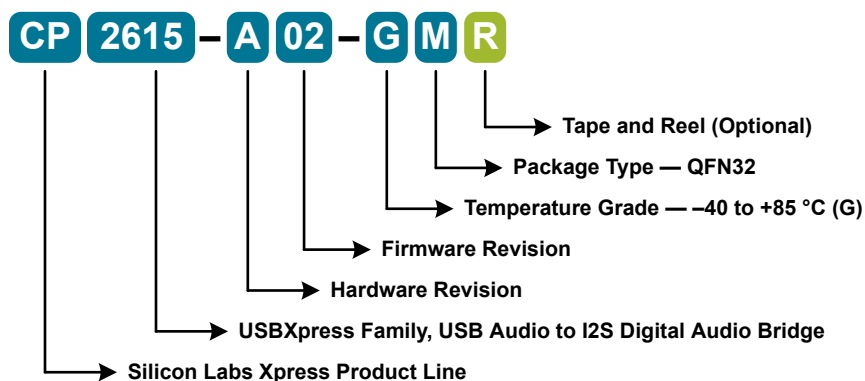


図 1.1. CP2615 部品番号

CP2615 デバイスには以下の特徴があります。

- ・ シングルチップ USB オーディオ-I²S デジタル・オーディオ・ブリッジ
 - ・ 統合された USB トランシーバ、外部抵抗不要
 - ・ 統合されたクロック、外部水晶不要
 - ・ オンチップ電圧レギュレータ：3.3 V 出力
 - ・ 統合された I²C で DAC/コーデックと通信
- ・ デジタル・オーディオ
 - ・ オーディオ・デバイス・リリース 1.0 の USB デバイス・クラス定義に準拠
 - ・ Windows/Android でネイティブにサポート（カスタム・ドライバ不要）
 - ・ Android USB ホスト・モード・オーディオ
 - ・ 44.1 kHz および 48 kHz のサンプリング・レート
 - ・ 同期または非同期エンドポイント
 - ・ 16 ビット・サンプル使用時の入力および出力同時オーディオ・ストリーム
 - ・ 24 ビット・サンプル使用時の入力または出カ方向オーディオ・ストリーム
- ・ USB 周辺装置機能コントローラ
 - ・ USB 仕様 2.0 準拠、フルスピード（12Mbps）
 - ・ USB サスペンド・ステートは、サスペンド・ピン経路でサポート
- ・ USB HID コンシューマ制御
 - ・ ボリュームおよびミュート同期用 USB HID コンシューマ制御に対応
- ・ 電力
 - ・ セルフパワーまたはバスパワー・モードに対応
- ・ その他の機能
 - ・ USB アクティブ・モードとアイドル・モードの両方において低電力で動作するように最適化されているため、デバイス電力供給アクセサリの開発が簡素化される
 - ・ 高度に統合された SoC によって外部部品表（BOM）コストと PCB 設置面積を削減
 - ・ 非水晶 USB の動作により、外部水晶が不要
 - ・ 内蔵のフラッシュ・メモリにデバイスのカスタマイズ・オプションが格納されるため、外部 EEPROM またはフラッシュ・ストレージが不要
 - ・ CP2614 MFi アクセサリ・デジタル・オーディオ・ブリッジとピン互換がある

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7.1 Revision 1.237

7.2 Revision 1.137

7.3 Revision 1.037

7.4 Revision 0.237

7.5 Revision 0.137

2. Electrical Specifications

2.1 Electrical Characteristics

2.1.1 Recommended Operating Conditions

Table 2.1. Global DC Electrical Characteristics ¹

| Parameter | Symbol | Test Condition | Min | Typ | Max | Units |
|---|----------|--|-----|------|-----|--------------|
| Digital Supply Voltage | V_{DD} | | 2.7 | — | 3.6 | V |
| Supply Current – Active Mode | | Sample rates: 44.1 kHz or 48 kHz Modes: • Play and Record (16-bit) • Play-only (24-bit or 16-bit) • Record-only (24-bit or 16-bit) | — | 20.2 | — | mA |
| Supply Current – Idle Mode | | Audio Play and Record not active | — | 7.2 | — | mA |
| Supply Current - Suspend Mode | | | — | 300 | — | μ A |
| Specified Operating Temperature Range | | | –40 | — | +85 | $^{\circ}$ C |
| Note: 1. V_{DD} = 2.7 to 3.6 V, –40 to +85 $^{\circ}$ C unless otherwise specified. | | | | | | |

2.1.2 I²S, I²C, GPIO and Alternate Function Pins

Table 2.2. I²S, I²C, GPIO and Alternate Function Pins DC Electrical Characteristics ¹

| Parameter | Symbol | Test Condition | Min | Typ | Max | Units |
|---|----------|--|----------------|----------------|---------|---------|
| Output High Voltage | V_{OH} | $I_{OH} = -10 \mu$ A, Port I/O push-pull | $V_{DD} - 0.1$ | — | — | V |
| | | $I_{OH} = -3$ mA, Port I/O push-pull | $V_{DD} - 0.7$ | — | — | |
| | | $I_{OH} = -10$ mA, Port I/O push-pull | — | $V_{DD} - 0.8$ | — | |
| Output Low Voltage | V_{OL} | $I_{OL} = 10 \mu$ A | — | — | 0.1 | V |
| | | $I_{OL} = 8.5$ mA | — | — | 0.6 | |
| | | $I_{OL} = 25$ mA | — | 1.0 | — | |
| Input High Voltage | V_{IH} | | 2.0 | — | — | V |
| Input Low Voltage | V_{IL} | | — | — | 0.8 | V |
| Input Leakage Current | | Weak Pull-Up Off | — | — | ± 1 | μ A |
| | | Weak Pull-Up On, $V_{IN} = 0$ V | — | 15 | 50 | |
| Note: 1. V_{DD} = 2.7 to 3.6 V, –40 to +85 $^{\circ}$ C unless otherwise specified. | | | | | | |

2.1.3 Reset

Table 2.3. Reset Electrical Characteristics ¹

| Parameter | Symbol | Test Condition | Min | Typ | Max | Units |
|--|--------|---|---------------------|-----|---------------------|---------------|
| RSTb Input High Voltage | | | $0.7 \times V_{DD}$ | — | — | V |
| RSTb Input Low Voltage | | | — | — | $0.3 \times V_{DD}$ | V |
| Minimum RSTb Low Time to Generate a System Reset | | | 15 | — | — | μs |
| RSTb Input Pullup Current | | RSTb = 0.0 V | — | 15 | 40 | μA |
| V_{DD} Ramp Time for Power On | | | — | — | 1 | ms |
| I ² C Slave Mode delay after reset | | RSTb high to first I ² C transaction | 100 | — | — | ms |

Note:
1. –40 to +85 °C unless otherwise specified.

2.1.4 Voltage Regulator

Table 2.4. Voltage Regulator Electrical Specifications ¹

| Parameter | Symbol | Test Condition | Min | Typ | Max | Units |
|---------------------|--------|------------------------------|-----|-----|------|-------|
| Input Voltage Range | | | 2.7 | — | 5.25 | V |
| Output Voltage | | Output Current = 1 to 100 mA | 3.0 | 3.3 | 3.6 | V |

Note:
1. –40 to +85 °C unless otherwise specified.

2.1.5 GPIO Output

Table 2.5. GPIO Output Specifications ¹

| Parameter | Symbol | Test Condition | Min | Typ | Max | Units |
|--------------------------|-------------|----------------|------------------------|-----------|------------------------|-------|
| GPIO.12/CLKOUT frequency | f_{OUT}^2 | | $f_{OUT} \times 0.985$ | f_{OUT} | $f_{OUT} \times 1.015$ | Hz |

Note:
1. –40 to +85 °C unless otherwise specified.
2. f_{OUT} is the CLKOUT frequency programmed by configuration.

2.1.6 I²S Digital Audio InterfaceTable 2.6. I²S Digital Audio Interface Specifications ¹

| Parameter | Symbol | Test Condition | Min | Typ | Max | Units |
|---|--------|------------------------|-----|--------|-----|--------|
| Resolution (output) | | | — | 16 | 24 | bits |
| Resolution (input) | | | — | 16 | 24 | bits |
| I2S_MCLK frequency | | | — | 12 | — | MHz |
| I2S_LRCLK frequency | | Sample Rate = 48 kHz | — | 48.0 | — | kHz |
| | | Sample Rate = 44.1 kHz | — | 44.118 | — | kHz |
| I2S_SCLK frequency | | | — | 3.429 | — | MHz |
| I2S_MCLK/I2S_LRCLK jitter | | Asynchronous endpoint | — | 140 | — | ps RMS |
| Note: 1. $V_{DD} = 2.7$ to 3.6 V, -40 to $+85$ °C unless otherwise specified. | | | | | | |

2.1.7 I²CTable 2.7. I²C Specifications ¹

| Parameter | Symbol | Test Condition | Min | Typ | Max | Units |
|---|--------|--|-----|-----|-----|-------|
| I2C_SCL frequency | | | — | 100 | — | kHz |
| Time to execute erase command | | I ² C slave mode | — | 65 | 100 | ms |
| Time to execute write command | | I ² C slave mode, 16-byte block | — | 0.8 | 1.2 | ms |
| Note: 1. $V_{DD} = 2.7$ to 3.6 V, -40 to $+85$ °C unless otherwise specified. | | | | | | |

2.1.8 Analog Output/Input

Table 2.8. Analog Output/Input Characteristics

| Parameter | Symbol | Test Condition ¹ | Min | Typ | Max | Units |
|--|--------|---|-----|-----|-----|-------|
| Analog Output | | | | | | |
| THD + Noise | | Playback resolution: 24 bits Asynchronous endpoint | — | -84 | — | dB |
| | | Playback resolution: 16 bits Asynchronous endpoint | — | -83 | — | dB |
| Analog Input | | | | | | |
| THD + Noise | | Playback resolution: 24 bits Asynchronous endpoint | — | -75 | — | dB |
| | | Playback resolution: 16 bits Asynchronous endpoint | — | -74 | — | dB |
| Note: 1. Common test conditions: <ul style="list-style-type: none"> • Sample rate — 48 kHz • Analog Output test signal — WAV file, 1 kHz, 0 dBFS • Analog Output measurement point — HEADPHONE jack (CP2615 Evaluation Board) • Analog Input test signal — 1 kHz, 1.0 VRMS • Analog Input stimulus point — LINE IN jack (CP2615 Evaluation Board) • Measurement bandwidth — 20 Hz – 20 kHz | | | | | | |

2.2 Absolute Maximum Ratings

Stresses above those listed in [2.1.1 Recommended Operating Conditions](#) may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. For more information on the available quality and reliability data, see the Quality and Reliability Monitor Report at <http://www.silabs.com/support/quality/pages/default.aspx>.

Table 2.9. Absolute Maximum Ratings

| Parameter | Symbol | Test Condition | Min | Max | Units |
|---|--------|-----------------------------|------|----------------|-------|
| Ambient Temperature Under Bias | | | -55 | 125 | C |
| Storage Temperature | | | -65 | 150 | C |
| Voltage on RSTb, GPIO, I ² S, I ² C, or VBUS Pins with respect to GND | | $V_{DD} \geq 2.2 \text{ V}$ | -0.3 | 5.8 | V |
| | | $V_{DD} < 2.2 \text{ V}$ | -0.3 | $V_{DD} + 3.6$ | |
| Voltage on VBUS with respect to GND | | $V_{DD} \geq 3.0 \text{ V}$ | -0.3 | 5.8 | V |
| | | V_{DD} not powered | -0.3 | $V_{DD} + 3.6$ | |
| Voltage on V_{DD} with respect to GND | | | -0.3 | 4.2 | V |
| Maximum Total Current through V_{DD} or GND | | | — | 500 | mA |
| Maximum Output Current Sunk by RSTb or any I/O pin | | | — | 100 | mA |

3. Functional Description

3.1 Audio Interfaces

3.1.1 Interface Signals

The CP2615 provides a Master Clock output and bidirectional I²S Master-mode interface for connection to an external converter. (For brevity, the term “converter” is used to represent a codec, DAC, or ADC.) The figure below shows the signals that comprise the audio interface.

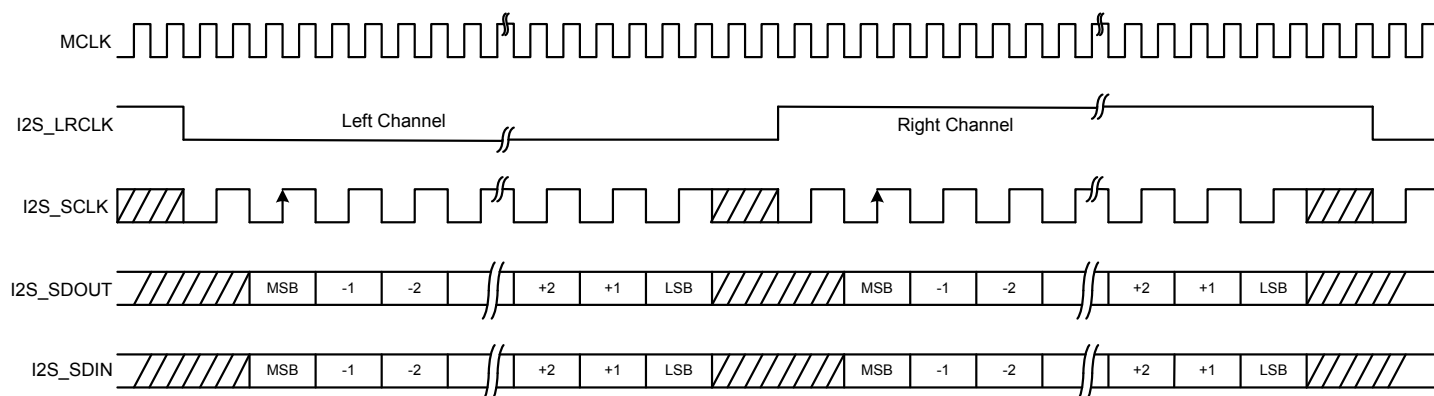


Figure 3.1. Audio Interface Signals

I2S_MCLK (output): The 12 MHz Master Clock output is typically used by oversampling audio converters to drive their internal analog-to-digital or digital-to-analog conversions.

I2S_LRCLK (output): The Left-Right Clock signal indicates which channel is currently being transferred on the interface. The I²S specification refers to this signal as WS (word select). The frequency of the I2S_LRCLK signal corresponds to the audio sample rate. The I2S_LRCLK and I2S_MCLK signals are derived from the same source, and I2S_LRCLK is an integer submultiple of I2S_MCLK. (Both of these attributes are typically required for proper codec operation.)

I2S_SCLK (output): The rising edge of Serial Clock indicates valid data on I2S_SDOUT and I2S_SDIN.

I2S_SDOUT (output): Serial Data Output from CP2615, typically connected to external DAC.

I2S_SDIN (input): Serial Data Input to CP2615, typically connected to external ADC.

The CP2615 operates in I²S Master Mode, and the I2S_LRCLK and I2S_SCLK signals are outputs from the CP2615. The external codec must operate in I²S Slave Mode. The I2S_LRCLK and I2S_SCLK signals are inputs for this mode.

3.1.2 Audio Sample Rates

The CP2615 supports audio sample rates of 44.1 kHz and 48 kHz. If both Playback and Record are used simultaneously, they must operate at the same sample rate. [Table 3.1 I2S_MCLK and I2S_LRCLK Supported Sample Rates on page 10](#) describes the relationship of I2S_MCLK and I2S_LRCLK for the supported sample rates:

Table 3.1. I2S_MCLK and I2S_LRCLK Supported Sample Rates

| I2S_MCLK Frequency | Nominal Sample Rate | I2S_MCLK/I2S_LRCLK Ratio | I2S_LRCLK Frequency |
|--------------------|---------------------|--------------------------|---------------------|
| 12.0 MHz | 48 kHz | 250 | 48000 Hz |
| | 44.1 kHz | 272 | 44,117.6 Hz |

3.1.3 Audio Sample Resolutions

The CP2615 can be configured to support any one of the following stereo Playback/Record modes:

- Playback and Record: 16-bit resolution
- Playback only: 24-bit or 16-bit resolution
- Record only: 24-bit or 16-bit resolution

3.1.4 Audio Endpoint Synchronization

USB audio endpoint synchronization is defined in Table 5.12 Synchronization Characteristics of the *Universal Serial Bus Specification Revision 2.0*. The CP2615 supports the synchronous or asynchronous endpoint synchronization methods for all input and output streaming configurations. In synchronous mode, the CP2615 adjusts the frequency of I2S_MCLK and I2S_LRCLK to match the rate at which Start-of-Frame (SOF) packets are received from the USB host. In asynchronous mode, the CP2615 does not adjust the I²S clocks and instead relies on the USB host to provide the synchronization based on implicit feedback from the input endpoint.

3.2 USB Function Controller and Transceiver

The Universal Serial Bus (USB) function controller in the CP2615 is a USB 2.0 compliant full-speed device with integrated transceiver and on-chip matching and pullup resistors. The USB function controller manages all control, audio, HID, and IO interface transfers between the USB host and the CP2615.

3.2.1 Endpoint Usage

The USB endpoints are allocated as follows:

Table 3.2. USB Endpoint Allocations

| Endpoint | Function |
|----------|--------------------------------|
| 0 | USB control |
| 1 | HID interface |
| 2 | Serial I/O interface |
| 3 | Audio streaming (configurable) |

3.2.1.1 USB Control Endpoint

The USB control endpoint is used for enumeration and normal USB control functions.

3.2.1.2 HID Interface Endpoint

The HID endpoint is an interrupt IN endpoint that is used to report Consumer Control (i.e. volume up, volume down, etc.) button presses.

3.2.1.3 Serial I/O Interface Endpoint

The Serial I/O endpoint is a bidirectional bulk interface that transfers either serial pass-through data with the CP2615 UART or I/O Protocol messages. A host application can use this interface to communicate with external devices or to interact with CP2615 general purpose I/O.

3.2.1.3.1 I/O Protocol

The CP2615 implements a simple messaging protocol that provides USB host applications a means for observing and controlling various I/O features. This custom protocol is named the I/O Protocol (IOP) and is implemented over the Serial I/O USB interface.

The I/O Protocol is a stateless, message based protocol that allows a USB host application to do the following:

- Query device identification information.
- Query GPIO configuration.
- Observe and control the GPIO.15-0 pins.
- Observe the analog pin GPIO.8/ADC.
- Receive autonomous notifications of GPIO/ADC changes.
- Perform small transfers on the I²C bus.
- Query error status of the UART.

Any pin configured as a GPIO output can be controlled by the I/O Protocol. This allows a USB host application to control visual indicators or other hardware connected to the CP2615.

The I/O Protocol supports two methods for observing GPIO.15-0 digital values and GPIO.8/ADC analog values. The USB host application can poll the CP2615 by sending an appropriate IOP message and receiving the response. Alternatively, the USB host application can request that IOP notification messages be sent automatically whenever specific GPIO pins change value. All GPIO pins, including those assigned to alternate functions, may be monitored over the IOP.

For more information, see *Application Note AN1139: CP2614 I/O Protocol*.

3.2.1.4 Audio Streaming Endpoint

This is an isochronous unidirectional or bi-directional audio streaming endpoint that carries USB digital audio data between the USB host and the CP2615. The audio streaming interface has several possible configurations.

3.2.2 USB Suspend

The USB Suspend and Resume modes are supported for power management of the CP2615 device. There are two optional Suspend output signals that can be used to control power switching to external circuitry. These are SUSPEND (active high) and SUSPENDb (active low). The CP2615 will enter Suspend mode when Suspend signaling is detected on the bus. On entering Suspend mode, the configured Suspend output signals are asserted. The Suspend signals are also asserted after a CP2615 reset until device configuration during USB enumeration is complete. The SUSPEND signal is logic high when the device is in the Suspend state, and logic low when the device is in the normal mode. The SUSPENDb signal has the opposite logic value of SUSPEND.

The CP2615 exits Suspend mode when any of the following occur: Resume signaling is detected or generated, a USB Reset signal is detected, or a device reset occurs. SUSPEND and SUSPENDb are weakly pulled to VIO in a high impedance state during a CP2615 reset. If this behavior is undesirable, a strong pulldown (10 Ω) can be used to ensure SUSPEND remains low during reset.

The output mode (push-pull or open drain) of the optional suspend output signals is controlled by the CP2615 configuration. Refer to the Configuration section for more details.

3.3 Asynchronous Serial Data Bus (UART) Interface

The CP2615 provides an asynchronous serial (UART) interface whose function is determined by the device configuration. When enabled, the UART interface provides a full duplex communication channel with a USB host application.

The UART interface consists of the GPIO.13/TX (transmit) and GPIO.14/RX (receive) data signals as well as the GPIO.11/RTS (ready to send) and GPIO.15/CTS (clear to send) flow control signals. These signals are described in [3.4.1.1 GPIO.15, 11—UART Flow-Control Pins \(RTS/CTS\)](#). Both the TX and RX signals must be configured to enable the UART interface. The use of RTS and CTS is optional depending on the use-case and baud rate.

The UART interface uses a fixed line configuration of 8 data bits, 1 stop bit and no parity (i.e., 8N1). Five common baud rates (115200, 57600, 38400, 19200 and 9600) are supported depending on the CP2615 functional configuration. Refer to the following sections for more information on the supported baud rates.

3.3.1 Serial Pass-Through Mode

When the CP2615 is configured for serial pass-through, the UART interface is used exclusively to provide a bi-directional data stream with a USB host application. The format and content of this communication stream is determined by the application and the CP2615 does not examine or interpret the data.

To ensure audio quality is not compromised, serial pass-through only supports low throughput communication. The table below summarizes the supported UART configurations for this mode. Communication over the serial pass-through may become unreliable if any other configuration is used.

Table 3.3. Supported Serial Pass-Through Configurations

| Configuration | Baud Rate | GPIO.11 / RTS | GPIO.15 / CTS |
|----------------|---------------------|----------------------|---------------|
| Any audio mode | 9600 | Optional | Optional |
| No audio mode | All supported rates | Required above 19200 | Optional |

3.4 GPIO

The CP2615 supports sixteen user-configurable GPIO pins. Each of these GPIO pins can be used as an input, open-drain output or push-pull output. GPIO pins are observed and controlled through the CP2615 I/O Protocol (IOP) which is accessed through the Serial I/O interface. Alternately, GPIO pins can be assigned to various alternate functions that are directly controlled by the CP2615. The available alternate functions are described in the following sections.

The function, mode and initial state of the sixteen GPIO pins is determined by the device configuration. More information regarding the configuration and usage of these pins is available in *AN1044: CP2615 Customization User Guide*.

Alternate function outputs can be configured as open-drain or push-pull.

3.4.1 Fixed Alternate Pin Functions (GPIO.15-8)

GPIO.15-8 pins have fixed alternate functions that are listed in the table below. Each pin may be individually configured as either a GPIO or its assigned alternate function. Alternate function pins are controlled directly by the CP2615, but their state can be read by the IOP protocol.

Table 3.4. GPIO.15-8 Alternate Functions

| Pin | Alternate Function |
|---------------------|------------------------------|
| GPIO.15 / CTS | UART CTS Flow-control Input |
| GPIO.14 / RX | UART Receive Data Input |
| GPIO.13 / TX | UART Transmit Data Output |
| GPIO.12 / CLKOUT | Clock Output |
| GPIO.11 / RTS | UART RTS Flow-control Output |
| GPIO.10 / RESETOUTb | Codec Reset Output |
| GPIO.9 / BUTTONS | Pushbutton Ladder Input |
| GPIO.8 / ADC | ADC Analog Input |

3.4.1.1 GPIO.15, 11—UART Flow-Control Pins (RTS/CTS)

The UART flow-control pins are used to prevent data loss by regulating the flow of UART data in either direction. These alternate functions are available when the CP2615 has been configured to enable the Serial I/O interface described in [3.3.1 Serial Pass-Through Mode](#). The pins are selected independently, so it is possible to have either or both configured.

GPIO.15/CTS, or Clear To Send, is an active-low input to the CP2615 and is driven logic low by an external UART device to signal that it can receive data. The CP2615 will halt transmitting data while CTS is pulled high.

GPIO.11/RTS, or Request To Send, is an active-low output from the CP2615, which indicates that the CP2615 is ready to accept data. The CP2615 will de-assert RTS whenever its internal buffers are nearly full. While RTS is high, the external UART device must stop transmitting to avoid data loss.

3.4.1.2 GPIO.14, 13—UART Data Pins (TX/RX)

The UART data pins should be selected whenever the CP2615 has been configured for serial pass-through. Both pins must be selected, even if only one direction is used.

GPIO.14/RX is the receive data pin for the CP2615 UART. Serial data received on this pin will be sent to the host if serial pass-through has been configured.

GPIO.13/TX is the transmit data pin for the CP2615 UART. Serial data from either the serial pass-through feature is transmitted on this pin.

3.4.1.3 GPIO.12—Programmable Clock Output (CLKOUT)

GPIO.12/CLKOUT is a configurable CMOS clock output. The clock output appears at the pin after the device enters High Power Mode. The clock output is removed from the pin when the device enters Low Power Mode or USB Suspend mode.

The output frequency is configurable through the use of a divider. When the divider is set to 0, the output frequency is 93.75 kHz. For divider values between 1 and 255, the output frequency is determined by the formula:

$$\text{CLKOUT}_{\text{freq}} = \frac{48 \text{ MHz}}{2 \times \text{divider}}$$

3.4.1.4 GPIO.10—Codec Reset Output (RESETOUTb)

GPIO.10/RESETOUTb is an active-low output that is typically used to drive the reset pin of the external codec. This pin is asserted (i.e. driven low) when the CP2615 enters Low Power mode, and can be controlled at other times via user-configurable I²C command strings. For more information, see [3.6.1.1 I²C Command Strings for Codec Configuration](#).

3.4.1.5 GPIO.9—Pushbutton Ladder Input (BUTTONS)

The CP2615 can be configured to report common consumer control buttons through the HID interface. When this feature is enabled, GPIO.9/BUTTONS can be used with a simple resistor ladder and up to fourteen pushbuttons to provide media button input to the CP2615. Additionally, HID media buttons can be connected as digital inputs to GPIO.7-0, which is described in [3.4.2.1 HID Media Buttons](#).

To sense button presses, the CP2615 periodically samples the input voltage on GPIO.9/BUTTONS. Once the input remains steady for a complete debounce period, the CP2615 converts the input value into a HID media button as determined by the device configuration. USB HID reports are then sent to the host as the button is pressed and when it is released.

The CP2615 divides the GPIO.9/BUTTONS input into sixteen equal sized ($V_{DD}/16$) slots numbered from 0 to 15. The center of each slot is given by the following equation, where n is the slot number.

$$V_n = \frac{V_{DD}}{32} \times (1 + 2 \times n)$$

Slots 1 through 14 can be assigned to any button listed in [Table 3.6 GPIO.7-0 Selectable Alternate Input Functions on page 17](#), while slots 0 and 15 are reserved for the no button pressed condition. Slots can also be left unassigned, in which case they are ignored.

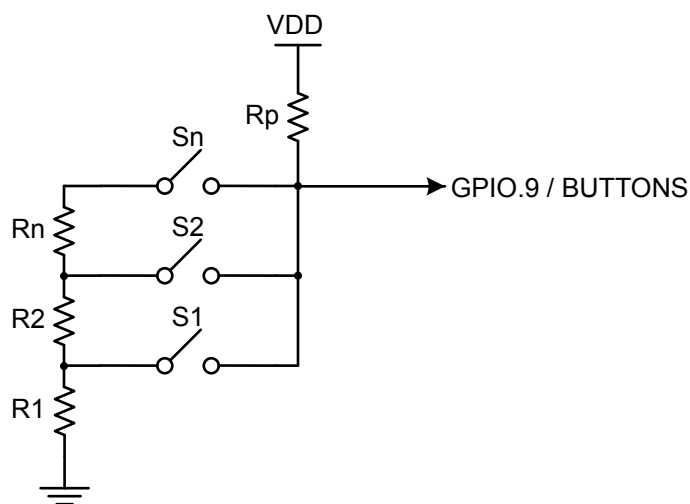


Figure 3.2. Example GPIO.9/BUTTONS Input Circuit

An example circuit for driving GPIO.9/BUTTONS is shown in the figure above. The circuit in the figure only shows three switches, but can easily be expanded by adding additional resistors and switches. While any switch is pressed a simple voltage divider of V_{DD} is formed and the voltage at GPIO.9/BUTTONS is easily calculated with the following equation.

$$V_{\text{buttons}} = V_{DD} \times \left(\frac{\sum_1^n R_i}{R_p + \sum_1^n R_i} \right)$$

The values of the resistor ladder should be selected so that the divider formed by each switch produces a voltage that is near the center of the switch's assigned slot. A set of resistor values for a fourteen button ladder are provided in the table, [Table 3.5 Resistor Values for Example GPIO.9/BUTTONS Circuit on page 16](#). To guarantee proper operation, 1% tolerance resistors should be used.

The example circuit in the figure above has some features worth noting. First, with no button pressed Rp holds GPIO.9/BUTTONS in slot 15 and the resistor ladder draws no current. Also, when multiple switches are pressed, the lowest numbered switch is recognized while the others are ignored. This is because the lowest switch effectively shorts the resistor ladder of the higher switches.

Table 3.5. Resistor Values for Example GPIO.9/BUTTONS Circuit

| Resistor | Value (kΩ) | Resistor | Value (kΩ) |
|----------|------------|----------|------------|
| Rp | 100 | — | — |
| R1 | 10.0 | R8 | 24.9 |
| R2 | 8.25 | R9 | 33.2 |
| R3 | 10.0 | R10 | 44.2 |
| R4 | 10.0 | R11 | 64.9 |
| R5 | 15.0 | R12 | 100 |
| R6 | 15.0 | R13 | 182 |
| R7 | 20.0 | R14 | 432 |

3.4.1.6 GPIO.8—ADC Analog Input (ADC)

The ADC Analog Input alternate function provides a low-rate analog measurement channel that is reported through the I/O Protocol. The analog value can be polled or automatically reported whenever the value change exceeds a programmable threshold. The CP2615 samples GPIO.8/ADC at approximately 50 samples per second and provides 10-bit resolution referenced to V_{DD} . This pin can be used to track a slow moving sensor value such as temperature.

3.4.2 Selectable Alternate Pin Functions (GPIO.7-0)

GPIO.7-0 pins have selectable alternate functions that can be mapped to any pin. The selectable alternate input functions and the selectable alternate output functions are listed in the tables below. These predefined functions can be assigned to GPIO.7-0 in any order and combination. Additionally, all output functions can be assigned to more than one pin if desired, and can be configured as open-drain or push-pull. Alternate function pins are controlled directly by the CP2615, but their state can be read by the IOP protocol.

Table 3.6. GPIO.7-0 Selectable Alternate Input Functions

| Alternate Input Name | Function |
|----------------------|---|
| PLAY_PAUSE | HID Media Button – Play/Pause |
| FFWD | HID Media Button – Scan Next Track |
| REW | HID Media Button – Scan Previous Track |
| MUTE | HID Media Button – Playback Mute |
| VOL+ | HID Media Button – Volume Increment |
| VOL- | HID Media Button – Volume Decrement |
| PLAY | HID Media Button – Play |
| STOP | HID Media Button – Stop |
| RECMUTE | Record Mute Toggle Button Input |
| PROFILE_SELECT | Cycle through audio profiles that have been configured or programmed by the host. |
| GESTURE | Implement multiple functions with one button. |

Table 3.7. GPIO.7-0 Selectable Alternate Output Functions

| Alternate Output Name | Function |
|-----------------------|---------------------------------------|
| SUSPEND | Suspend Mode (active high) |
| SUSPENDb | Suspend Mode (active low) |
| LOWPWR | Low Power Mode (active high) |
| LOWPWRb | Low Power Mode (active low) |
| RMUTE | Audio Record is Muted (active high) |
| RMUTEb | Audio Record is Muted (active low) |
| PBMUTE | Audio Playback is Muted (active high) |
| PBMUTEb | Audio Playback is Muted (active low) |

3.4.2.1 HID Media Buttons

The CP2615 can be configured to report common consumer control buttons through the HID interface. These active low inputs are debounced by the CP2615 and are used to generate the HID reports on both the leading and trailing edges of a button push. The supported HID usages are indicated in [Table 3.6 GPIO.7-0 Selectable Alternate Input Functions on page 17](#). These inputs should be connected to momentary pushbuttons through an external pull-up resistor. Note that buttons can also be connected to the CP2615 using GPIO.9/BUTTONS as described in [3.4.1.5 GPIO.9—Pushbutton Ladder Input \(BUTTONS\)](#).

3.4.2.2 Record Mute Toggle Button

This active low input is debounced by the CP2615 and is used to toggle the internal audio record mute state. The CP2615 record mute state is toggled on a low-to-high transition. This input should be connected to a momentary pushbutton through an external pull-up resistor.

3.4.2.3 PROFILE_SELECT

Configuring a GPIO or buttons (resistor ladder) switch as a PROFILE_SELECT input allows the user to select between multiple profiles that are typically used to specify codec register writes that implement different equalization or audio effect settings. The CP2615 can be configured with up to three fixed audio profiles, and a fourth profile can be dynamically programmed by the host.

Each time the PROFILE_SELECT button is pressed, the next non-blank profile string is applied in round robin fashion ([0]>[1]>[2]>[0]). Blank profile strings (i.e. containing only the 00 terminator) are skipped. The currently-selected profile is saved to nonvolatile memory and persists across CP2615 reset and power-cycle events. The currently-selected profile will be applied when audio streaming starts.

3.4.2.4 GESTURE

The CP2615 recognizes four gestures (i.e. distinct types of GESTURE button press):

- Long press
- Single click
- Double click
- Triple click

Each of these four gestures can be assigned to the any of these Alternate Input Functions that are described in [Table 3.6 GPIO.7-0 Selectable Alternate Input Functions on page 17](#):

- HID Media button functions (PLAY_PAUSE, FFWD, REW, MUTE, VOL+, VOL-, PLAY, STOP)
- RECMUTE
- PROFILE_SELECT

3.4.2.5 SUSPEND, SUSPENDb

These complimentary outputs are asserted while the CP2615 is in USB Suspend mode. The CP2615 enters USB Suspend mode when it is powered and USB is disconnected or USB activity is stopped by the connected USB host. This situation occurs if the CP2615 accessory is self-powered (such as with a battery) and a connected USB host goes into standby mode (powers down) or USB is disconnected. If the accessory is device powered, then USB Suspend mode will not be used. The CP2615 enters a very low power state while in USB Suspend mode, and the SUSPEND output signal(s) can be used to switch power to other circuitry in the accessory.

3.4.2.6 LOWPWR, LOWPWRb

These complimentary outputs are asserted whenever the CP2615 is in low power mode. The CP2615 enters low power mode when both the audio and serial I/O interfaces are idle. The LOWPWR output signal(s) can be used to switch power to other circuitry in the accessory in order to save power.

3.4.2.7 RMUTE, RMUTEb

The CP2615 asserts these complimentary outputs whenever it is muting the audio record channel. These signals reflect the state of the CP2615 audio record mute and can be used to drive a visual indicator for user feedback or drive the mute control of a microphone pre-amp.

3.4.2.8 PBMUTE, PBMUTEb

The CP2615 asserts these complimentary outputs whenever the host has commanded the CP2615 to mute the audio playback channel. These signals can be used to drive mute controls in the playback circuitry or to provide user feedback by driving a visual indicator.

3.5 Configuration

The CP2615 has an extensive set of configurable features and attributes. To streamline the product development process, the CP2615 Evaluation Kit provides tools that enable users to easily customize and program the CP2615 configuration parameters to meet the requirements of their system.

In the production environment, the CP2615 configuration can be programmed in-situ using an industry-standard I²C EEPROM Programmer or equivalent. Customers can also order devices that are pre-programmed with their customized configuration.

Some of the configuration options of the CP2615 do not have a fixed length. For example, the manufacturer name and product name strings do not have a fixed length. Also, the codec configuration data can be variable length. While the CP2615 does not enforce any fixed length on these individual fields, the total configuration size can be a maximum of 2800 bytes. The baseline configuration length with no codec configuration and minimal identification strings is about 575 bytes. The CP2615 customization tool will show you the size of the configuration.

3.5.1 Configuration Parameters

The CP2615 configuration parameters can be grouped as follows:

- Device IDs and Strings
- Power Options
- Audio Options
- GPIO and Alternate Functions

The following sections provide an overview of each of these categories. For more information on CP2615 configuration parameters, refer to *AN1044: CP2615 Customization User Guide*.

3.5.1.1 Device IDs and strings

The following IDs and strings are configurable:

- USB Vendor and Product IDs
- USB Manufacturer, Product, and Serial Number strings

3.5.1.2 Power Options

The following power options are configurable:

- Power Mode (Bus-Powered or Self-Powered)
- Maximum Power Consumption

3.5.1.3 HID Consumer Control Buttons

- HID Consumer Control Buttons
 - Play
 - Stop
 - Scan Next Track (Transport Right)
 - Scan Previous Track (Transport Left)
 - Play/Pause
 - Mute
 - Volume Increment (Louder)
 - Volume Decrement (Softer)

3.5.1.4 Audio Options

The following audio playback and record options are selectable:

- No playback or record
- Playback only, 16-bit resolution
- Playback only, 24-bit resolution
- Playback only, 24-bit and 16-bit resolution
- Record only, 16-bit resolution
- Record only, 24-bit resolution
- Record only, 24-bit and 16-bit resolution
- Playback and record, 16-bit resolution
- Synchronization mode: synchronous or asynchronous

To facilitate using the CP2615 with various codecs devices, the configuration contains elements for specifying volume and mute behavior, as well as I²C commands for initializing and dynamically configuring the codec.

3.5.1.5 GPIO and Alternate Functions

GPIO pins can be configured to have fixed or selectable functions, as as a general purpose input or output. For more information about fixed alternate pin functions, see [3.4.1 Fixed Alternate Pin Functions \(GPIO.15-8\)](#) and for selectable pin functions see [3.4.2 Selectable Alternate Pin Functions \(GPIO.7-0\)](#).

3.6 I²C Interface

The I²C (inter-integrated-circuit) bus is a de facto standard two-wire digital interface. For detailed information on the I²C standard, see the NXP I²C Bus Specification and User Manual.

The CP2615 operates in I²C Standard Mode at the nominal frequency of 100 kbits/s. For proper operation, the SCL (clock) and SDA (data) lines require external pullup resistors that are sized to ensure that the SCL/SDA rise times satisfy the requirements of all devices on the I²C bus. Improperly sized pullup resistors may cause data corruption or bus lockup.

The state of the CFGMODEb input pin when RSTb becomes deasserted determines whether the CP2615 operates in Normal Mode as an I²C Master (CFGMODEb = high), or in Configuration Mode as an I²C Slave (CFGMODEb = low).

3.6.1 CP2615 I²C Operation in Normal Mode

In Normal Mode the CP2615 provides the following I²C functionality:

- Execute pre-configured I²C write transactions in response to various system events (e.g. bootup, audio stream start/stop, volume/mute commands, audio profile switching, etc).
- Support I²C pass-through operation, enabling the host to initiate read or write transactions with I²C slave devices.

3.6.1.1 I²C Command Strings for Codec Configuration

The CP2615 supports a number of configurable I²C command strings that are typically used to initialize and configure the codec and other I²C slave devices in the system.

Table 3.8 Command Strings on page 21 lists the various I²C strings, describes when the strings are applied, and indicates if the given I²C string requires a zero-terminator byte (0x00) to identify the end of all subcommands.

Table 3.8. Command Strings

| I ² C Command String | Description | Requires Zero Terminator? |
|--|---|---------------------------|
| Codec Initialize | Executed on power mode transition from low to high. | Yes |
| Codec High To Low | Executed on power mode transition from high to low. | Yes |
| Audio Start | Executed when audio play/record streaming starts. | Yes |
| Audio Stop | Executed when audio play/record streaming stops. | Yes |
| Volume Set Prefix (Left) Volume Set Prefix (Right) | I ² C bytes sent prior to writing the playback volume setting byte. | No |
| Volume Set Suffix (Left) Volume Set Suffix (Right) | I ² C bytes sent after writing the playback volume setting byte. | Yes |
| Get Mute Prefix | I ² C bytes sent prior to reading the playback mute setting byte. | Yes |
| Set Mute Prefix | I ² C bytes sent prior to writing the playback mute setting byte. | No |
| Set Mute Suffix | I ² C bytes sent after writing the playback mute setting byte. | Yes |
| Set Sample Rate (48 kHz) Set Sample Rate (44.1 kHz) | Executed when host sets the sample rate. | Yes |
| Profile (0, 1, 2) | Currently-selected profile is applied when audio streaming starts. Clicking PROFILE_SEL button selects and applies next profile. | Yes |

Each I²C command string consists of a length byte followed by an array of bytes containing one or more subcommands. As indicated in Table 3.8 Command Strings on page 21, most I²C command strings must also be terminated with 0x00. The value of the length byte includes the size of the subcommand array and zero terminator, but not the length byte itself.

The maximum length of any one I²C command string is 2000 bytes, including the length byte and the zero terminator byte. The length byte should be set to the maximum value of 254 if the string is longer than 254 bytes. The maximum size of the entire CP2615 configuration (which includes all I²C command strings, USB descriptors and other device configuration info) is 4608 bytes.

The subcommands which comprise an I²C command string are composed of a one-byte ASCII-encoded subcommand token followed by the number of data bytes specific to that token. The ASCII-encoded tokens and their associated arguments are shown in Table 3.9 ASCII-encoded Tokens and Associated Arguments on page 21.

Table 3.9. ASCII-encoded Tokens and Associated Arguments

| Token | Operation | Arguments (Binary) |
|-------------|---|--|
| “W” 0x57 | I ² C Write (Write one or more bytes) | U8: Number of bytes to write (size of array to be written) U8: Slave address U8[]: Bytes to be written |
| “R” 0x52 | I ² C Read (Read one or more bytes) | U8: Number of bytes to read U8: Slave address |

| Token | Operation | Arguments (Binary) |
|---------------------------|---|--|
| “P” 0x50 | I ² C Stop (Issue stop condition) | None |
| “C” 0x43 | Assert codec reset output (RESE-TOUTb) | None |
| “c” 0x63 | Deassert codec reset output (RESE-TOUTb) | None |
| “D” 0x44 | Delay | U8: Delay in ms U8: Reserved |
| “B” 0x42 | Perform CP2615 reboot | U8: waitForTransactionComplete If zero reboot immediately, else reboot when transaction is complete |
| “G” 0x47 (A02 only) | Set or clear GPIO pin(s) | U16: Mask (bitmapped, e.g. bit 0 = GPIO.0) Selects which GPIOs to write: <ul style="list-style-type: none"> • 0: GPIO state is unchanged • 1: GPIO written with corresponding Value bit U16: Value (bitmapped, e.g. bit 0 = GPIO.0) GPIO values to write if corresponding Mask bit is set. |

The ‘W’ (write) and ‘R’ (read) operations always begin with an I²C start condition. The I²C stop condition must be explicitly specified for both read and write operations.

3.6.1.2 Example I²C Subcommands

This section contains examples of typical I²C subcommands. The examples use these conventions:

- Tokens are shown as ASCII characters, e.g. 'W'
- Binary data is shown as hex (e.g. 0x01)
- <SLA> represents the left-justified slave address

The following are examples typical I²C subcommands.

Write 0x44 to register 0x01 of slave device:

```
0x06 'W' 0x03 <SLA> 0x01 0x44 'P'
```

Read 2 bytes from register 0x55 of slave device, using stop/start between Write/Read transactions:

```
0x09 'W' 0x02 <SLA> 0x01 'P' 'R' 0x02 'SLA' 'P'
```

Read 2 bytes from register 0xAA of slave device, using repeated start between Write/Read transactions:

```
0x09 'W' 0x01 <SLA> 0xAA 'R' 0x02 'SLA' 'P'
```

Delay 20 ms (20 = 0x14):

```
0x06 'D' 0x14 0x00
```

(A02 only) Set GPIO.15 high, GPIO.8 high, GPIO.1 low. (For this operation, Mask = 1000 0001 0000 0010 and Value = 1xxx xxx1 xxxx xx0x). The un-masked bits can be written to any value, e.g.

```
0x06 'G' 0x81 0x02 0x81 0x00 'P'
```

```
0x06 'G' 0x81 0x02 0xFF 0xFD 'P'
```

3.6.1.3 I²C Pass-Through

The CP2615 I/O Protocol allows USB host applications to issue I²C write and read operations to I²C slave devices, and to the CP2615's internal user-accessible ROM. For more information on the I/O protocol, see [3.2.1.3.1 I/O Protocol](#).

Using pass-through mode, the host can also perform the following write and read operations which are recognized by the CP2615 and are not passed through to the physical I²C bus:

Table 3.10. Write/Read Operations in Pass-through Mode (A02 only)

| CP2615 Slave Address (binary) | Register Address (hex) | Write Operation | Read Operation |
|-------------------------------|------------------------|-----------------------------------|----------------------------------|
| 1111 00x | FFFB | n/a | Read CP2615 firmware revision |
| 1111 000 | FFFC | Erase entire configuration area | n/a |
| 1111 000 | FFFD | Write Config lock | Read Config lock |
| 1111 000 | FFFE | Reset CP2615 | n/a |
| 1111 000 | 0000-17FF | Write (entire configuration area) | Read (entire configuration area) |
| 1111 001 | 1400-17FF | Write (audio profile area only) | Read (audio profile area only) |

3.6.2 CP2615 I²C Operation in Configuration Mode

The state of the CFGMODEb input pin at the conclusion of the device reset state determines whether the CP2615 operates normally (CFGMODEb = high) or enters Configuration Mode (CFGMODEb = low). In Configuration Mode, the CP2615 emulates an I²C flash EEPROM; all other device functionality is disabled. The CP2615 remains in Configuration Mode until it is reset or power-cycled. Refer to the following figure for typical configuration connections.

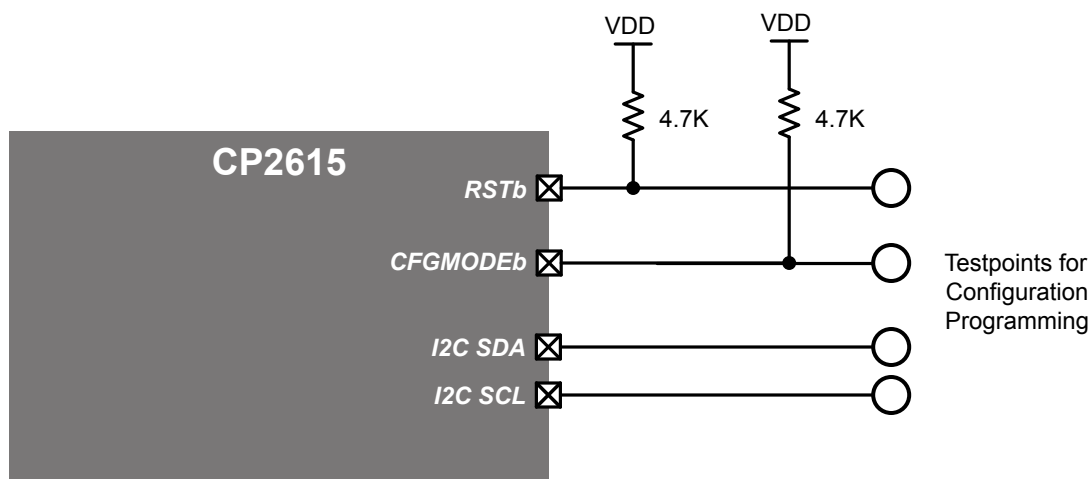


Figure 3.3. Typical I²C Configuration

The following sequence puts the CP2615 into Configuration Mode, after which an external I²C Master can be used to program the CP2615 configuration.

- Drive CFGMODEb and RSTb low (device power can be applied before or after this step)
- Delay at least 15 μ s (the minimum RSTb low time)
- Drive RSTb high
- Delay at least 100 ms

The configuration block consists of 2048 bytes of non-volatile flash memory mapped to address range 0x0000-0x07FF. Two bytes are used in I²C Read and Write transactions to represent the address within the configuration block.

The CP2615 7-bit I²C Slave Address is 0011000. The corresponding 8-bit values for the CP2615 slave address plus the I²C Write/Read bit are 0x30 (Write) and 0x31 (Read).

CP2615 code execution is temporarily halted during the execution of memory erase and write operations. If the external I²C Master cannot tolerate NAKs or does not support retries, it must implement the appropriate delays after issuing I²C erase and write commands.

3.6.2.1 I²C Write Transactions

To prevent inadvertent flash erasure or corruption, each Write transaction must contain the flash keys (0xA5, 0xF1) between the address MSB/LSB and the block of data to be written. Write transactions with invalid flash keys will be ignored. The maximum number of data bytes that can be written per Write transaction is 62 bytes. The format of the Write transaction is:

Table 3.11. Write Transaction Format

| | | | | | | | |
|-------|---------------|---------|---------|------|------|---------------------|------|
| Start | 0x30 SLA+W | AddrMSB | AddrLSB | 0xA5 | 0xF1 | Data[0] ... Data[n] | Stop |
|-------|---------------|---------|---------|------|------|---------------------|------|

3.6.2.2 I²C Read Transactions

The entire configuration block can be read with a single Read transaction (if the external I²C Master is capable) or by using multiple Read transactions of smaller size. The format of the Read transaction is as follows:

Table 3.12. Read Transaction Format

| | | | | | | | | |
|-------|---------------|----------------|----------------|------|-------|---------------|------------------------|------|
| Start | 0x30 SLA+W | Address MSB | Address LSB | Stop | Start | 0x31 SLA+R | Data[0] ... Data[n] | Stop |
|-------|---------------|----------------|----------------|------|-------|---------------|------------------------|------|

3.6.2.3 Special Operations

In Configuration Mode, the CP2615 recognizes these addresses outside of the configuration block address range:

Table 3.13. Read CP2615 Firmware Revision

| | | | | | | | | |
|-------|------|------|------|------|-------|------|-------------------------------|------|
| Start | 0x30 | 0xFF | 0xFB | Stop | Start | 0x31 | Firmware Version Number | Stop |
|-------|------|------|------|------|-------|------|-------------------------------|------|

Table 3.14. Erase the Configuration

| | | | | | | |
|-------|------|------|------|------|------|------|
| Start | 0x30 | 0xFF | 0xFC | 0xA5 | 0xF1 | Stop |
|-------|------|------|------|------|------|------|

Table 3.15. Lock the Configuration

| | | | | | | |
|-------|------|------|------|------|------|------|
| Start | 0x30 | 0xFF | 0xFD | 0xA5 | 0xF1 | Stop |
|-------|------|------|------|------|------|------|

Table 3.16. Read the Configuration Lock Byte

| | | | | | | | | |
|-------|------|------|------|------|-------|------|---------------------|------|
| Start | 0x30 | 0xFF | 0xFD | Stop | Start | 0x31 | Config Lock Byte | Stop |
|-------|------|------|------|------|-------|------|---------------------|------|

Table 3.17. Reset CP2615

| | | | | |
|-------|------|------|------|------|
| Start | 0x30 | 0xFF | 0xFE | Stop |
|-------|------|------|------|------|

3.6.2.4 Configuration Programming Example

The following sequence illustrates the actions required of an external I²C Master when programming the CP2615 configuration. The sequence programs the new configuration data in blocks of 16 bytes, which is a typical size used by I²C EEPROM programmers.

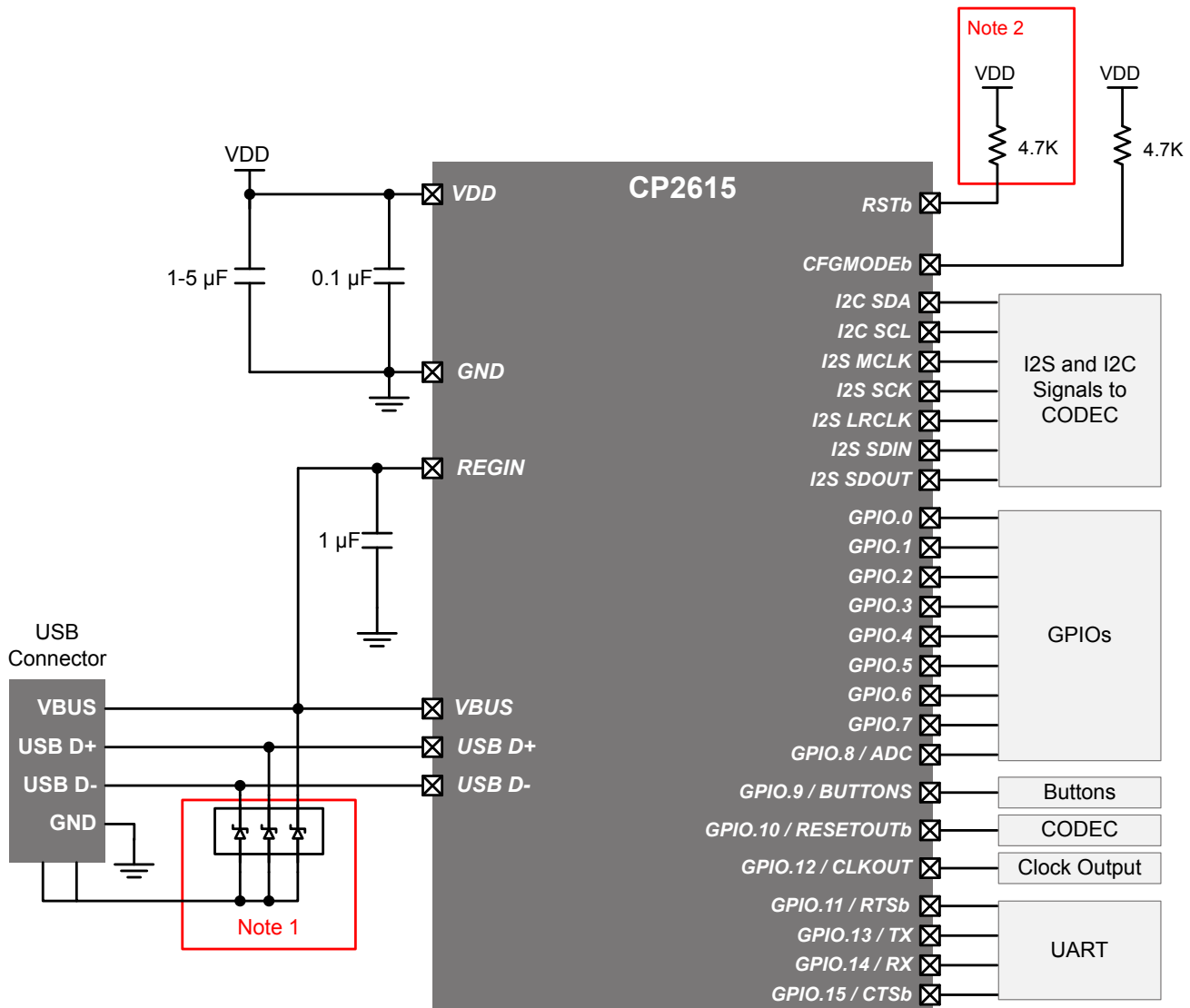
- Put the CP2615 into Configuration Mode.
- Read the Configuration Lock Byte to ensure it is 0xFF (i.e. unlocked).
- Erase the configuration.
- Delay while configuration is being erased (see [2.1.7 I²C](#)).
- Read the Configuration Block to ensure all bytes are 0xFF.
- For each block of 16 bytes to be written:
 - Execute Write transaction containing flash keys and 16 bytes of data.
 - Delay while configuration data is being written.
 - Execute 16-byte Read transaction to verify data.
- Lock the configuration. (optional).
- To return the CP2615 to normal operation, reset or power-cycle the device.

3.7 Voltage Regulator and Power

The CP2615 includes an internal voltage regulator that can be configured to operate in one of several modes. This allows it to be powered from an ordinary USB host or be self-powered.

3.7.1 USB Bus-Powered Connection

A typical connection diagram of the device in a USB bus-powered application using the regulator is shown in the figure below. When enabled, the voltage regulator output appears on the VDD pin and can be used to power external devices. See 2.1.4 Voltage Regulator for the voltage regulator electrical characteristics.



Note 1 : Avalanche transient voltage suppression diodes compatible with Full-speed USB should be added at the connector for ESD protection. Use Littelfuse p/n SP0503BAHT or equivalent.

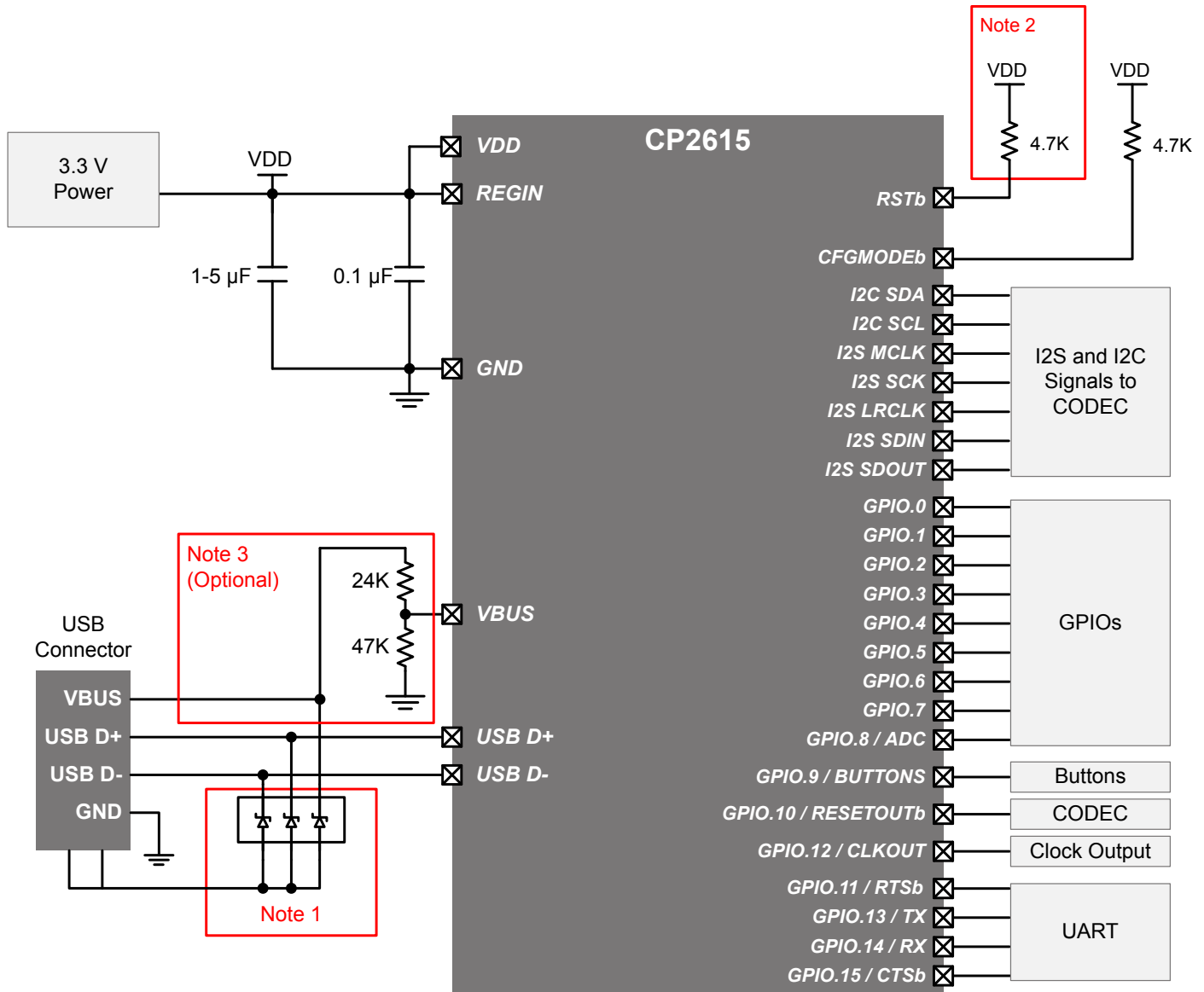
Note 2 : An external pull-up is not required, but can be added for noise immunity.

Figure 3.4. USB Bus-Powered Configuration

3.7.2 USB 3.3 V Self-Powered Connection

Alternatively, if 3.0 to 3.6 V power source is supplied to the VDD pin, the CP2615 can function as a USB self-powered device with the voltage regulator bypassed. For this configuration, the REGIN input should be tied to VDD to bypass the voltage regulator. A typical connection diagram showing the device in a USB self-powered application with the regulator bypassed is shown in the figure below.

The USB max power and power attributes descriptor must match the device power usage and configuration. See application note AN1044: CP2615 Customization User Guide for information on how to customize USB descriptors for the CP2615.



Note 1 : Avalanche transient voltage suppression diodes compatible with Full-speed USB should be added at the connector for ESD protection. Use Littelfuse p/n SP0503BAHT or equivalent.

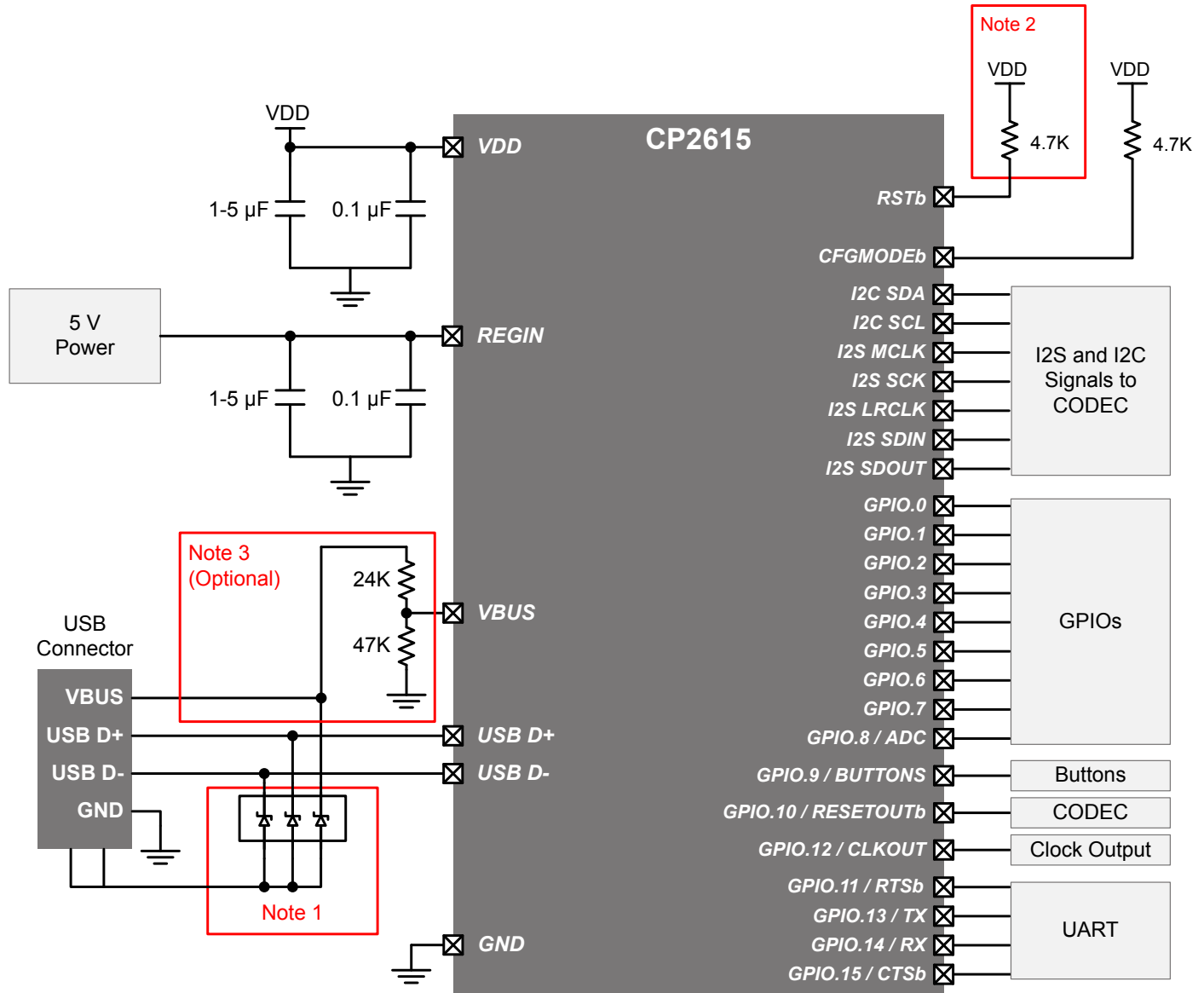
Note 2 : An external pull-up is not required, but can be added for noise immunity.

Note 3 : For self-powered systems where VDD may be unpowered when VBUS is connected to 5 V, a resistor divider (or functionally-equivalent circuit) on VBUS is required to meet the absolute maximum voltage on VBUS specification in the Electrical Characteristics section.

Figure 3.5. USB Self-Powered Application with Regulator Bypassed

3.7.3 USB 5 V Self-Powered Connection

To use the regulator to provide VDD in a self-powered application, use the configuration shown in the diagram below. If REGIN may be unpowered while VBUS is 5 V, a resistor divider (or functionally equivalent circuit) described in Note 3 of the figure is required to meet the absolute maximum voltage on VBUS specification in 2.2 Absolute Maximum Ratings.



Note 1 : Avalanche transient voltage suppression diodes compatible with Full-speed USB should be added at the connector for ESD protection. Use Littelfuse p/n SP0503BAHT or equivalent.

Note 2 : An external pull-up is not required, but can be added for noise immunity.

Note 3 : For self-powered systems where VDD may be unpowered when VBUS is connected to 5 V, a resistor divider (or functionally-equivalent circuit) on VBUS is required to meet the absolute maximum voltage on VBUS specification in the Electrical Characteristics section.

Figure 3.6. USB 5 V Self-Powered Application with Regulator Used

4. Pin Definitions

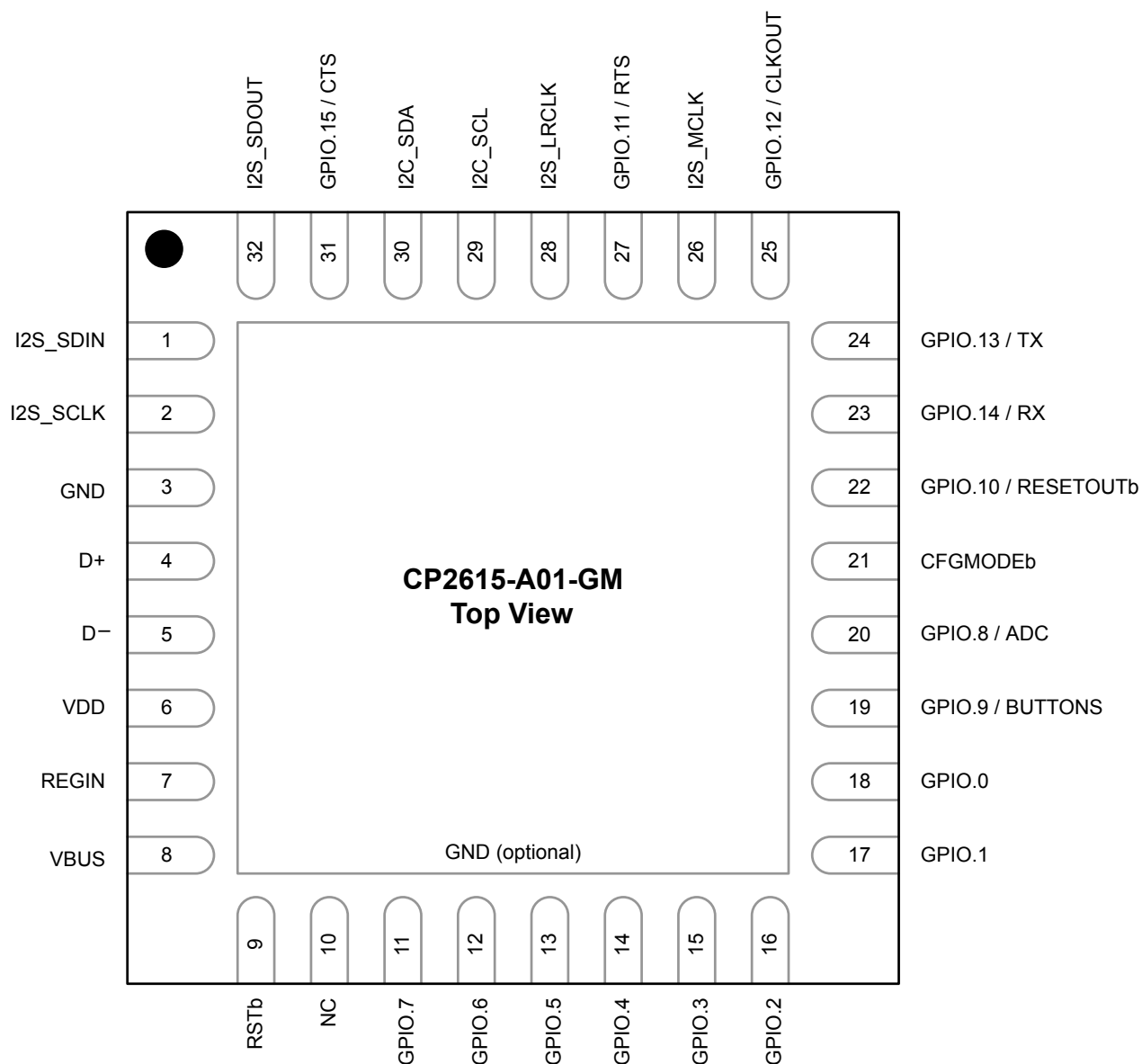


Figure 4.1. CP2615 QFN32 Pinout Diagram (Top View)

Table 4.1. CP2615 Pin Descriptions

| Pin # | Name | Function | Description ¹ |
|-------|----------|----------------------------|---|
| 1 | I2S_SDIN | Digital Input ² | I ² S interface: Serial data input |
| 2 | I2S_SCLK | Digital Output | I ² S interface: Serial clock output |
| 3 | GND | | Ground. Must be tied to system ground. |
| 4 | D+ | Digital Input/Output | USB D+ |
| 5 | D- | Digital Input/Output | USB D- |

| Pin # | Name | Function | Description ¹ |
|-------|-----------|-----------------------------------|--|
| 6 | VDD | Power Input | Power supply voltage Input |
| | | Power Output ² | Output of the on-chip voltage regulator |
| 7 | REGIN | Power Input | Input to the on-chip voltage regulator |
| 8 | VBUS | Digital Input | VBUS Sense Input. This pin should be connected to the Accessory Power signal from a USB host, or to the VBUS signal from a USB host. |
| 9 | RSTb | Digital Input/Output ² | Device Reset. Open-drain output of internal POR or VDD monitor. An external source can initiate a system reset by driving this pin low for the time specified in 2.1.3 Reset . |
| 10 | NC | | This pin should be left unconnected |
| 11 | GPIO.7 | Digital Input/Output ² | GPIO or selectable alternate function |
| 12 | GPIO.6 | Digital Input/Output ² | GPIO or selectable alternate function |
| 13 | GPIO.5 | Digital Input/Output ² | GPIO or selectable alternate function |
| 14 | GPIO.4 | Digital Input/Output ² | GPIO or selectable alternate function |
| 15 | GPIO.3 | Digital Input/Output ² | GPIO or selectable alternate function |
| 16 | GPIO.2 | Digital Input/Output ² | GPIO or selectable alternate function |
| 17 | GPIO.1 | Digital Input/Output ² | GPIO or selectable alternate function |
| 18 | GPIO.0 | Digital Input/Output ² | GPIO or selectable alternate function |
| 19 | GPIO.9 | Digital Input/Output ² | GPIO |
| | BUTTONS | Analog Input | Analog input for sensing buttons connected via resistor ladder |
| 20 | GPIO.8 | Digital Input/Output ² | GPIO |
| | ADC | Analog Input | General purpose analog input, readable via I/O protocol |
| 21 | CFGMODEb | Digital Input | Configuration Mode input. If CFGMODEb is low when RSTb becomes deasserted, CP2615 enters Configuration Mode. |
| 22 | GPIO.10 | Digital Input/Output ² | GPIO |
| | RESETOUTb | Digital Output ² | Output signal controllable via I ² C command string (typically connected to codec reset pin) |
| 23 | GPIO.14 | Digital Input/Output ² | GPIO |
| | RX | Digital Input | UART receive data |
| 24 | GPIO.13 | Digital Input/Output ² | GPIO |
| | TX | Digital Output | UART transmit data |
| 25 | GPIO.12 | Digital Input/Output ² | GPIO |
| | CLKOUT | Digital Output | Configurable clock output |
| 26 | I2S_MCLK | Digital Output | I ² S interface: Master clock output |
| 27 | GPIO.11 | Digital Input/Output ² | GPIO |
| | RTS | Digital Output | UART RTS flow-control output |
| 28 | I2S_LRCLK | Digital Output | I ² S interface: Left/right clock output |
| 29 | I2C_SCL | Digital Input/Output ² | I ² C interface: Serial clock input/output |

| Pin # | Name | Function | Description ¹ |
|-------|------------|-----------------------------------|--|
| 30 | I2C_SDA | Digital Input/Output ² | I ² C interface: Serial data input/output |
| 31 | GPIO.15 | Digital Input/Output ² | GPIO |
| | CTS | Digital Input | UART CTS flow-control input |
| 32 | I2S_SDOOUT | Digital Output ² | I ² S interface: Serial data output |

Note:

1. GPIO: General Purpose Input or Output.
2. For the specified function, pin can be left unconnected if not used
3. Requires external pullup resistor to V_{DD} .

5. QFN32 Package Specifications

5.1 QFN32 Package Dimensions

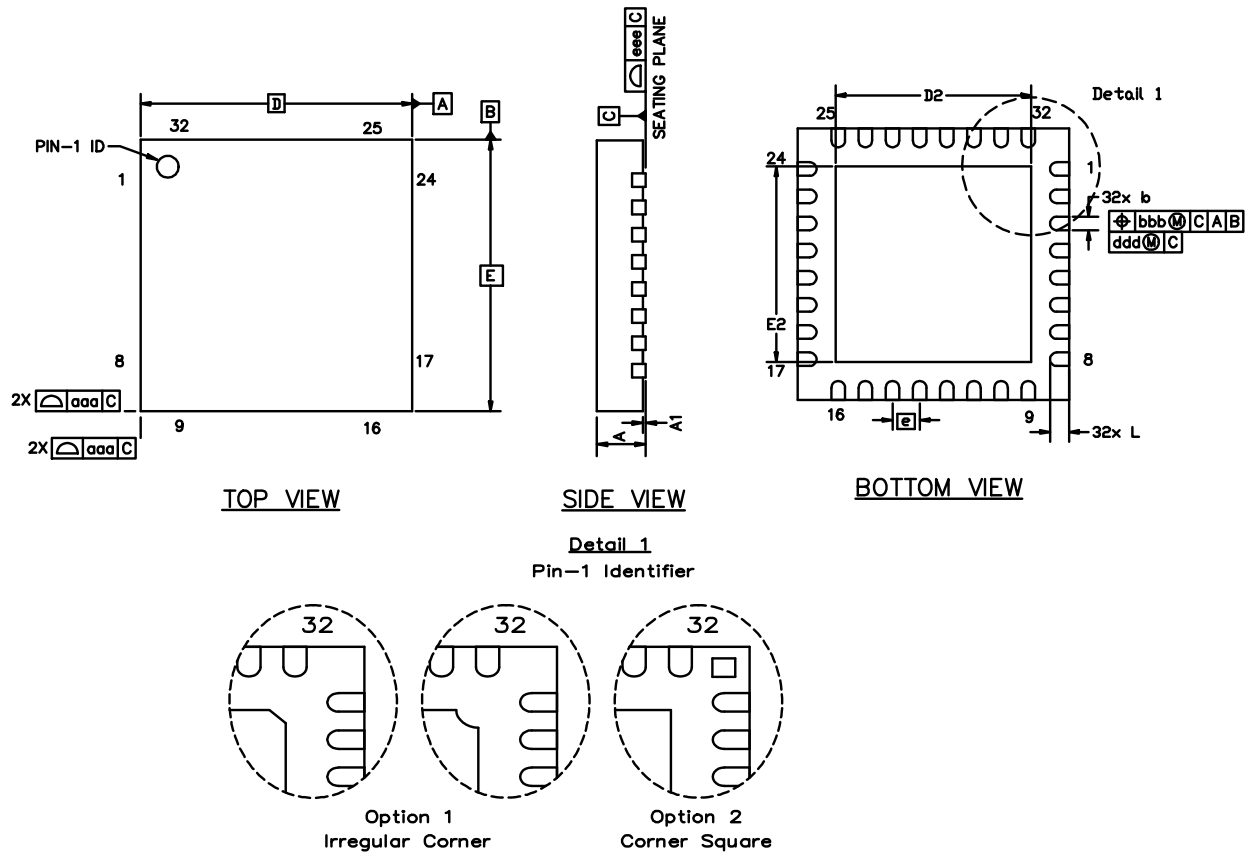


Figure 5.1. QFN32 Package Drawing

Table 5.1. QFN32 Package Dimensions

| Dimension | Min | Typ | Max |
|-----------|-----------|------|------|
| A | 0.80 | 0.85 | 0.90 |
| A1 | 0.00 | 0.02 | 0.05 |
| b | 0.18 | 0.25 | 0.30 |
| D | 5.00 BSC. | | |
| D2 | 3.20 | 3.30 | 3.40 |
| e | 0.50 BSC. | | |
| E | 5.00 BSC. | | |
| E2 | 3.20 | 3.30 | 3.40 |
| L | 0.35 | 0.40 | 0.45 |
| aaa | — | — | 0.10 |

| Dimension | Min | Typ | Max |
|-----------|-----|-----|------|
| bbb | — | — | 0.10 |
| ddd | — | — | 0.05 |
| eee | — | — | 0.08 |

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220, variation VHHD except for custom features D2, E2, and L which are toleranced per supplier designation.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

5.2 QFN32 PCB Land Pattern

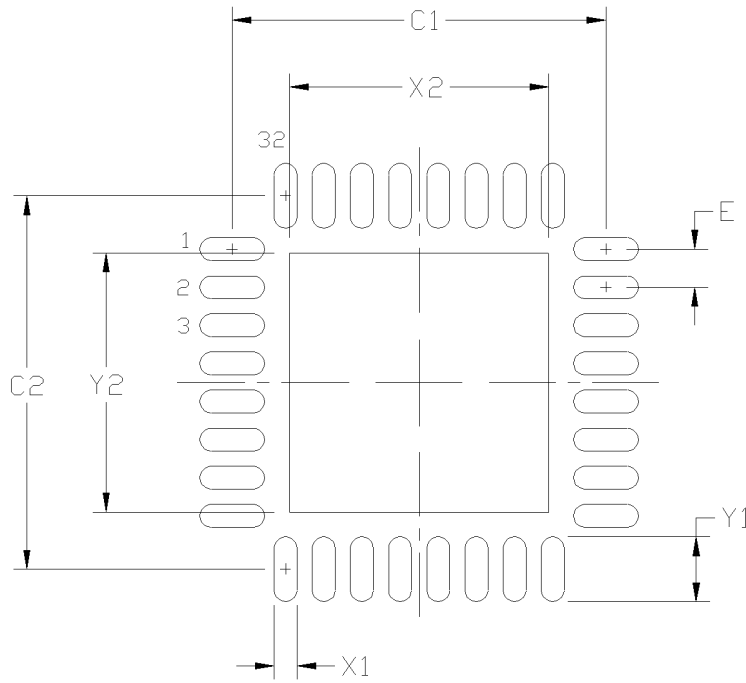


Figure 5.2. QFN32 Recommended PCB Land Pattern

Table 5.2. QFN32 PCB Land Pattern Dimensions

| Dimension | Min | Max |
|-----------|----------|------|
| C1 | 4.80 | 4.90 |
| C2 | 4.80 | 4.90 |
| E | 0.50 BSC | |
| X1 | 0.20 | 0.30 |
| X2 | 3.20 | 3.40 |
| Y1 | 0.75 | 0.85 |
| Y2 | 3.20 | 3.40 |

| Dimension | Min | Max |
|---|-----|-----|
| Note: | | |
| General | | |
| <ol style="list-style-type: none"> All dimensions shown are in millimeters (mm) unless otherwise noted. This Land Pattern Design is based on the IPC-7351 guidelines. | | |
| Solder Mask Design | | |
| <ol style="list-style-type: none"> All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 μm minimum, all the way around the pad. | | |
| Stencil Design | | |
| <ol style="list-style-type: none"> A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release. The stencil thickness should be 0.125 mm (5 mils). The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads. A 3x3 array of 1.0 mm square openings on 1.2 mm pitch should be used for the center ground pad. | | |
| Card Assembly | | |
| <ol style="list-style-type: none"> A No-Clean, Type-3 solder paste is recommended. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components. | | |

5.3 QFN32 Package Marking

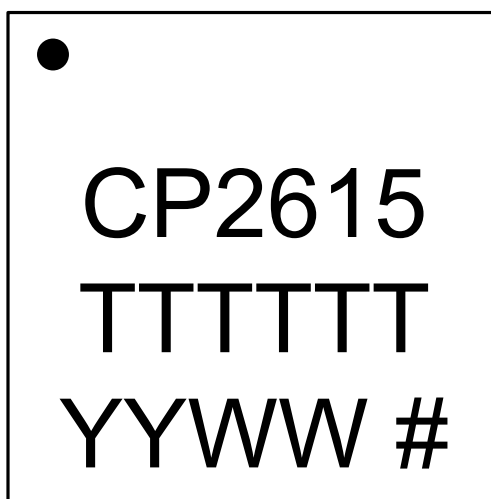


Figure 5.3. QFN32 Package Marking

The package marking consists of:

- TTTTTT – A trace or manufacturing code.
- YY – The last two digits of the assembly year.
- WW – The two-digit work week when the device was assembled.
- # – Part Hardware Revision (i.e. A).

6. Relevant Application Notes

The following Application Notes are applicable to the CP2615. Please visit <http://www.silabs.com> to access the latest version of the application notes and accompanying software.

- *AN1044: CP2615 Customization User Guide*—this application note describes the steps required to customize a CP2615 fixed-function USB device.
- *AN1139: CP2615 I/O Protocol*

7. Revision History

7.1 Revision 1.2

March, 2018

- Updated front page block diagram.
- Updated part number revision to A02 in [1. Feature List and Ordering Information](#)
- Corrected GPIO.15/CTS behavior description in [3.4.1.1 GPIO.15, 11—UART Flow-Control Pins \(RTS/CTS\)](#)
- Added two audio options in [3.5.1.4 Audio Options](#).
- Added [3.4.2.3 PROFILE_SELECT](#).
- Added [3.4.2.4 GESTURE](#).
- Updated [3.6 I²C Interface](#).
- Updated [3.6.1 CP2615 I²C Operation in Normal Mode](#) (formerly, Normal Mode: CP2615 as I2C Master)
- Updated [3.6.1.1 I²C Command Strings for Codec Configuration](#).
- Updated [3.6.1.2 Example I²C Subcommands](#) (formerly, Example I2C Command Strings).
- Updated [3.6.1.3 I²C Pass-Through](#).
- Updated [3.6.2.3 Special Operations](#).
- Updated package marking in [5.3 QFN32 Package Marking](#).
- Added AN1139 to [6. Relevant Application Notes](#).

7.2 Revision 1.1

April 11th, 2017

- Corrected the regulator output voltage listed in [1. Feature List and Ordering Information](#).
- Filled in all TBDs in [2. Electrical Specifications](#).
- Updated the typical specification for Supply Current - Suspend Mode and removed Supply Current - USB Pull-up in [2.1.1 Recommended Operating Conditions](#).
- Updated the note in [2.1.8 Analog Output/Input](#) to specify measurements are taken in asynchronous mode.
- Updated all references to *AN1044: CP2615 Customization User Guide* to refer to the correct document.
- Updated the maximum string sizes in [3.6.1.1 I²C Command Strings for Codec Configuration](#).
- Updated the synchronization option descriptions in [3.1.4 Audio Endpoint Synchronization](#) and [3.5.1.4 Audio Options](#).
- Updated the title for this section: [3.7.2 USB 3.3 V Self-Powered Connection](#).

7.3 Revision 1.0

October 14th, 2016

- Revision updated with no changes to the document.

7.4 Revision 0.2

May 18th, 2016

- Added all content except for the front page and features.

7.5 Revision 0.1

May 13th, 2016

- Initial release.

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