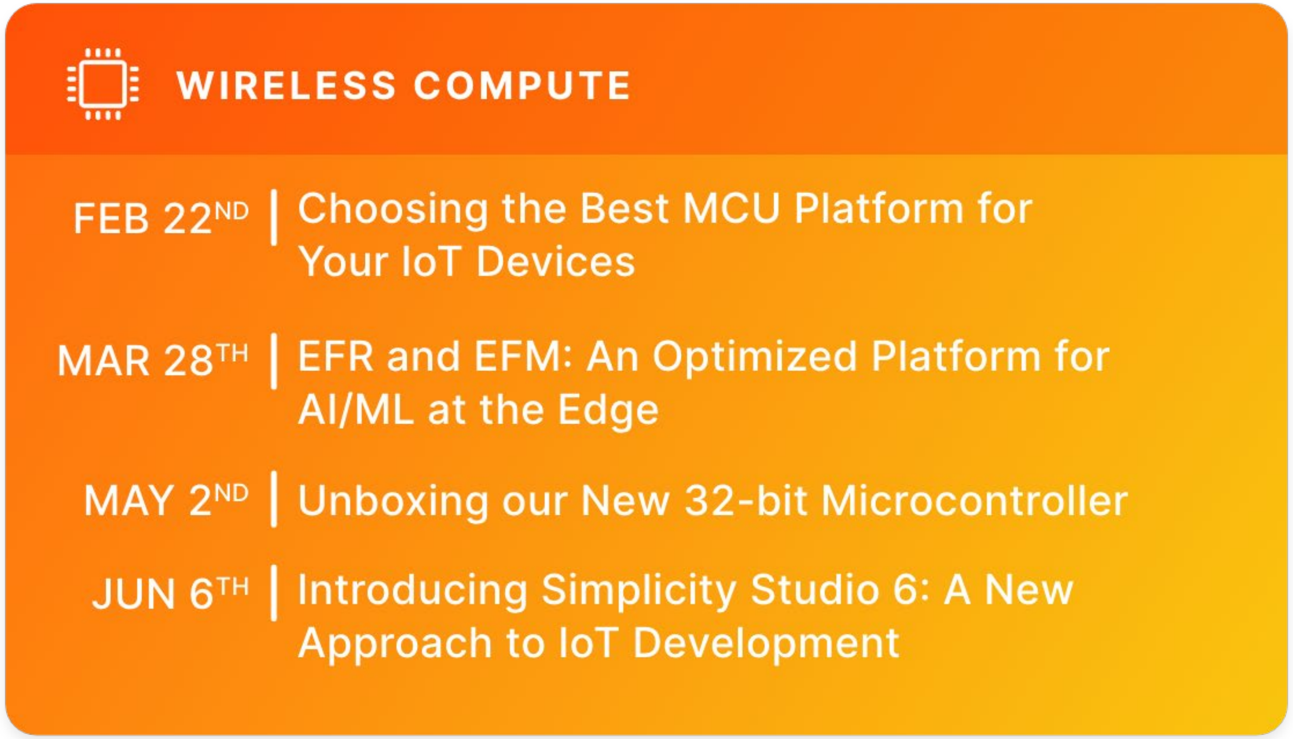
Presentation Will Begin Shortly

4:00



WIRELESS COMPUTE

FEB 22ND | Choosing the Best MCU Platform for Your IoT Devices

MAR 28TH | EFR and EFM: An Optimized Platform for AI/ML at the Edge

MAY 2ND | Unboxing our New 32-bit Microcontroller

JUN 6TH | Introducing Simplicity Studio 6: A New Approach to IoT Development

Welcome

Choosing the Best MCU Platform for Your IoT Devices

Jayanth Krishna – Staff Product Manager, I&C BU

tech talks

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Agenda

01 Key sub-systems in a MCU

02 Construct and considerations for each of the sub-systems

03 Q&A

04 Mapping of Silicon Labs' portfolio to MCU categories

05 Q&A

MCU Building Blocks

The Sub-systems

Processor Core

- 8/16/32 bit
- DMIPS / MHz
- Power efficiencies

Memory

- Volatile / Nonvolatile
- On chip / Off chip
- Code / Data

Peripherals

- Analog
- Digital / Serial i/fs
- Display

Wireless

- Short range / Long range
- <1GHz, 2.4GHz, 5GHz

Security

- PSA Level
- Within the CPU
- Isolated sub-system

AI/ML

- Matrix& Math acceleration
- Neural net support
- Power Optimization

Processor Cores

DESIGN CONSIDERATIONS

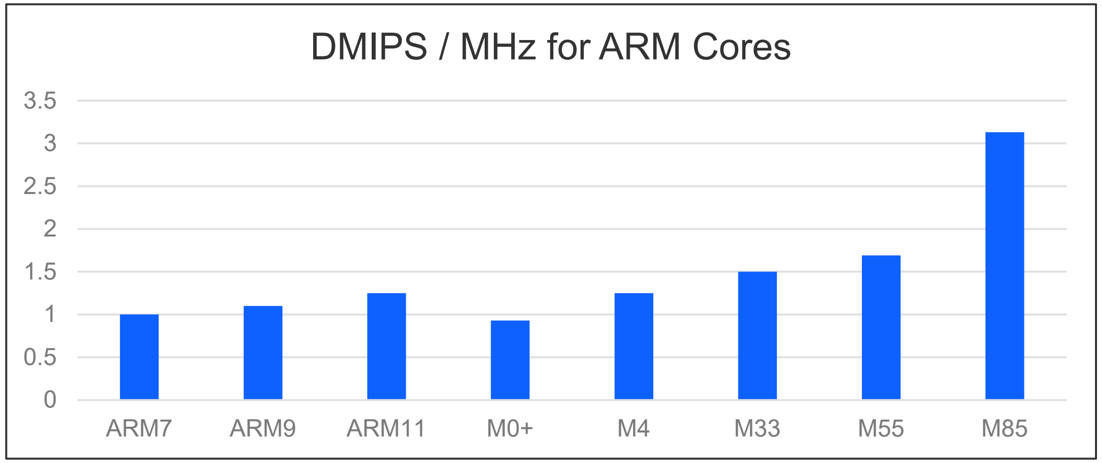
Different MCU architectures are better suited for certain applications

- Each architecture has a key set of applications that it is best suited for

General Considerations:

- Computational requirements
- Power Consumption
- Interface or Peripheral Needs

ARM CORE PERFORMANCE



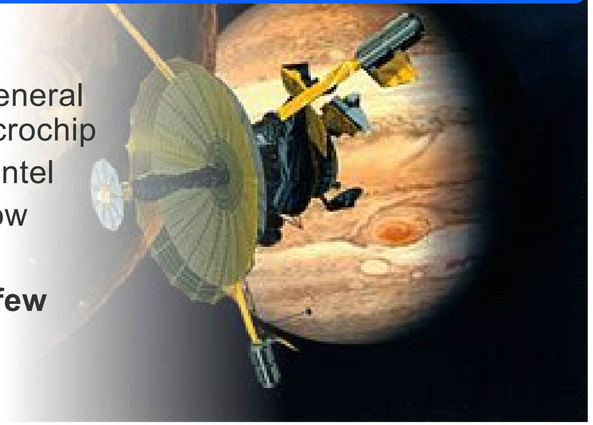
8-BIT ARCHITECTURES

Core Architectures

- PIC - Developed in 1975 by General Instruments now owned by Microchip
- 8051 – Developed in 1980 by Intel
- AVR – Developed by Atmel, now owned by Microchip

Operating Frequencies: 10s to few x00s of MHz

Performance: ~1 MIPS/MHz



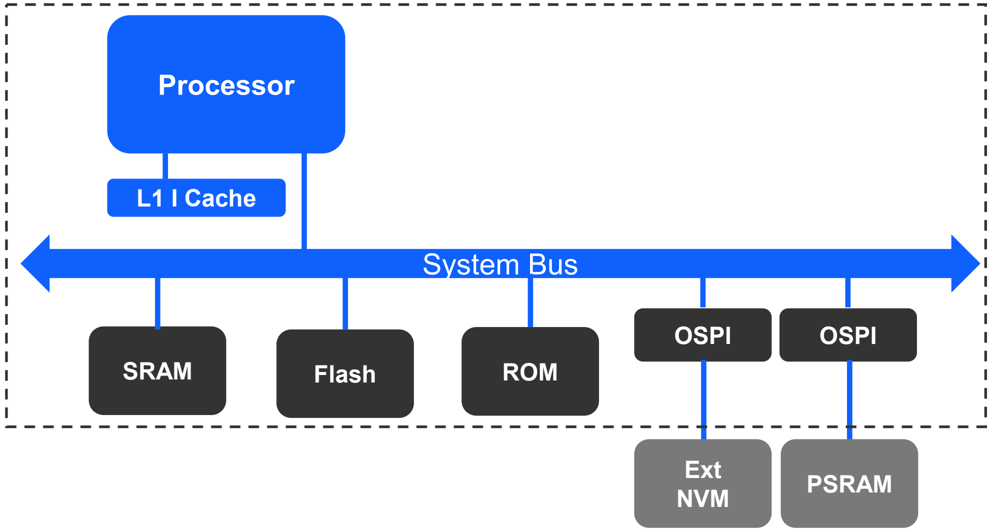
32-BIT ARCHITECTURES

Core Architectures

- ARM – Developed by ARM, most prevalent 32-bit core in embedded designs
- RISC V – Open source architecture, gaining traction with key partnerships in semiconductor industry
- PIC32 / AVR32 – Proprietary architectures owned by Microchip

Operating Frequencies: 10s of MHz to ~1GHz

Memory Sub-system

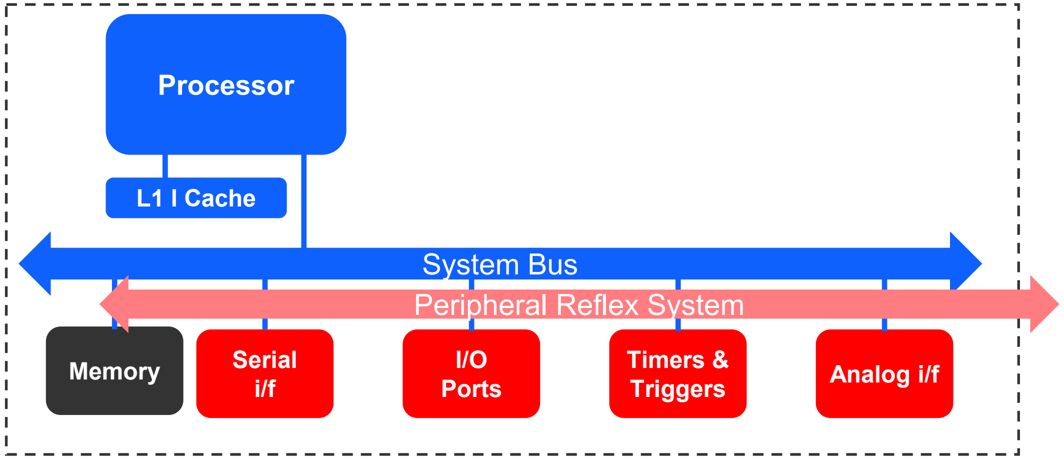


- **Cache:** On chip, volatile. Used for extremely quick fetches of data / instruction
- **Embedded Flash**: Non-volatile memory (NVM), used to store code, certain parameters & keys.
- **ROM:** NVM which is used only for code; immutable, patching options available.
- **SRAM** – Volatile, typically used for data, execution is an option
- **External Memory**: Outside of chip boundary, flash and RAM variants available.

Key Considerations

- Power consumption
  - Executing from on-chip NVM extremely efficient, external storage crosses chip boundaries and hence higher power consumption; ROM is the most power efficient code memory
- Latency
  - Fetch (code / data) from external interfaces takes more time
- Determinism
  - When crossing chip boundaries, contentions are possible and execution jitter is certain.
- Size & Extensibility
  - On chip memories are fixed size; need to factor growth as applications become complex, more so in long lifetime products.
  - OTA is a significant contributor even if compressed
  - External memories provide extensibility

Peripheral Sub-system

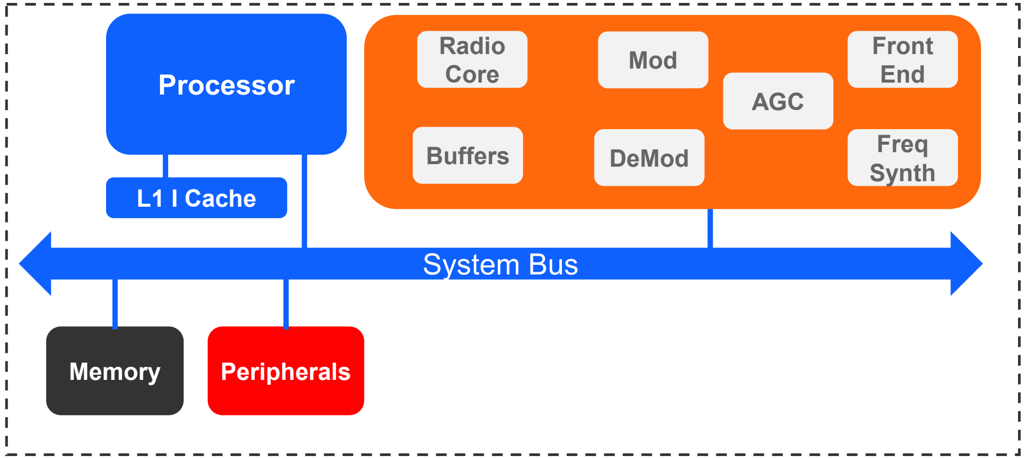


- **Series i/f:** USART, I2C, I3C, USB, CAN, Ethernet etc
- **I/O Ports**: KBD Scanner, External interrupts, GPIO, Reset, Wakeup
- **Timers & Triggers:** Timers, Protocol timers**,** LE Timer, Watchdog, RTC, PWM
- **Analog i/f** – ADC, DAC, Cap Touch, ACMP, OpAmp

Key Considerations

- Speeds and Feeds
  - Specific interfaces based on external components on the design. Instances, data rates and throughputs.
- Power Mode
  - Availability in different power save modes to optimize system power across different application scenarios.
- Simultaneous availability
  - Concurrency based on use case, flexibility of system for different designs (Pin map)
- Software enablement
  - Drivers & s/w tools
- Relative interaction
  - Sense and actuate : What external inputs trigger what outputs to the external world?
  - Latency and power during such interaction

Wireless Sub-system

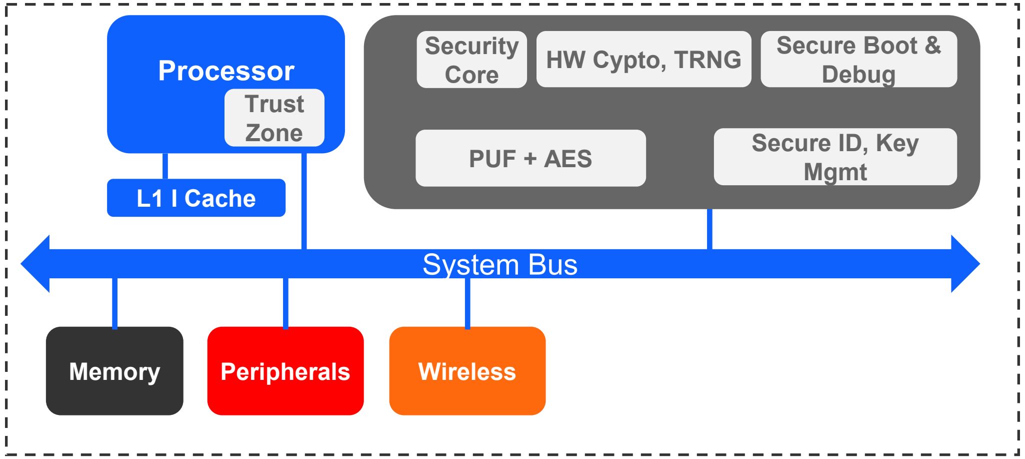


- **Front End:** Power amp (0-20 dBm), LNA, RX/TX Frontend
- **Freq Synthesizer**: Spectrum of operation, Modulation scheme, Freq Deviation
- **AGC:** Automatic gain control to maximize SNR
- **Mod & Demod** – Modulation and demodulation scheme handling like (G)FSK, ASK / OOK, (O)QPSK etc
- **Buffers**: Stores both Tx and Rx data using RAM
- **Radio Core**: Brain of the radio sub-system, interaction with the main system, configuration management

Key Considerations

- Spectrum of operation
  - ISM Bands are most popular in IoT
  - 2.4 GHz, < 1 GHz
- Deployment Eco System
  - Municipal infrastructure, Smart Buildings, Retail environment, Smart Home
- Range
  - Determines the spectrum to be used and the Transmit power.
  - Topology – Mesh vs Point to point, protocol oriented
- Simultaneous availability
  - Radio considerations and co-existence mechanisms determine the ability of device to live in different networks simultaneously

Security Sub-System

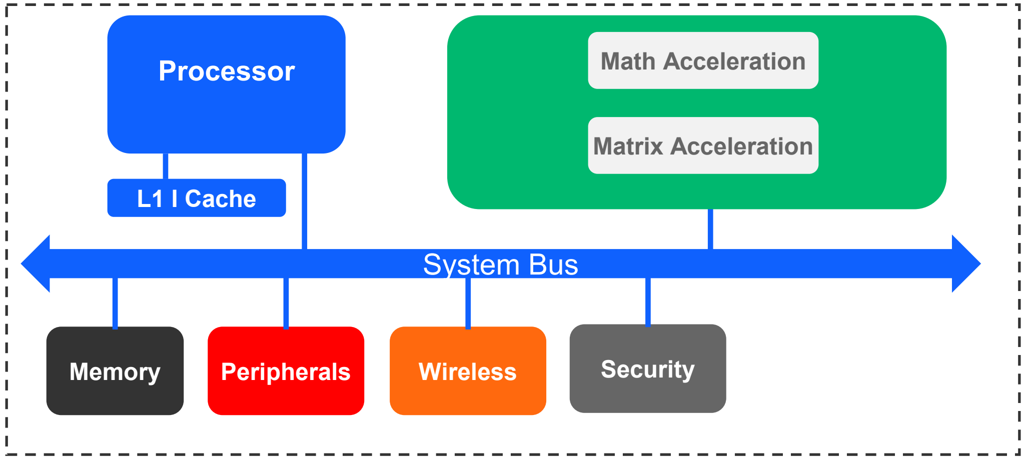


- **Secure Boot & Debug :** Running verified images, ROM code used as root of trust; validation of OTA images. Debug port locked, needs token to read flash
- **Secure ID & Key Mgmt :** Sub-system has private key unique to the device and not known to other sub-systems. PUF, Wrapped keys, PUF, processor never sees key in unwrapped**.**
- **TRNG**: Based on physical process, used as seed for DRBG
- **Security Core**: Brain of the sub-system, interaction with the main system, configuration management
- **Trust Zone**: Split application into secure and non-secure code

Key Considerations

- Attack Vectors
  - Remote attacks, Local Logical Glitch attack, Local Physical DPA (Differential Power Analysis), Flash Extraction, Physical attack on the Die
- Regulatory Requirements
  - Geography and industry (medical, industrial) dependent requirements
  - Ex: US Cyber trust mark, ETSI EN 303 645, RED, Singapore regulations
- Protocol standard based requirements
  - Intent vis-à-vis the language
  - Ex: Matter calls for specific requirements on secure boot and identity etc
- Future Considerations
  - Longevity of the devices and evolution of attacks

AI/ML Sub-System

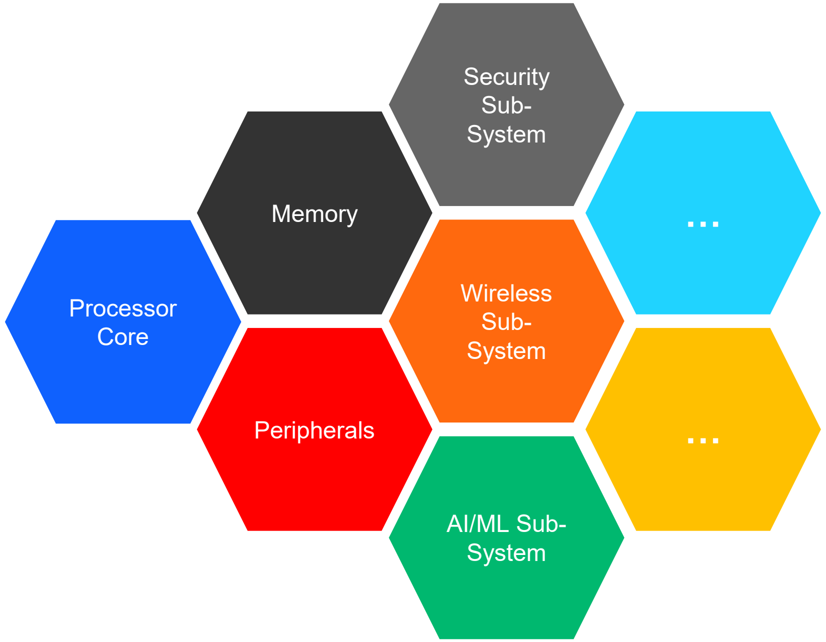


- **Matrix Acceleration:** Floating point acceleration for neural nets & specific algorithms like MUSIC
  - Matrix multiplication
  - Element-wise matrix multiplication
  - Matrix addition
  - Power series generation
  - Convolution
- **Math Acceleration:** Cordic functions like trigonometric identities, log, sqrt etc

Key Considerations

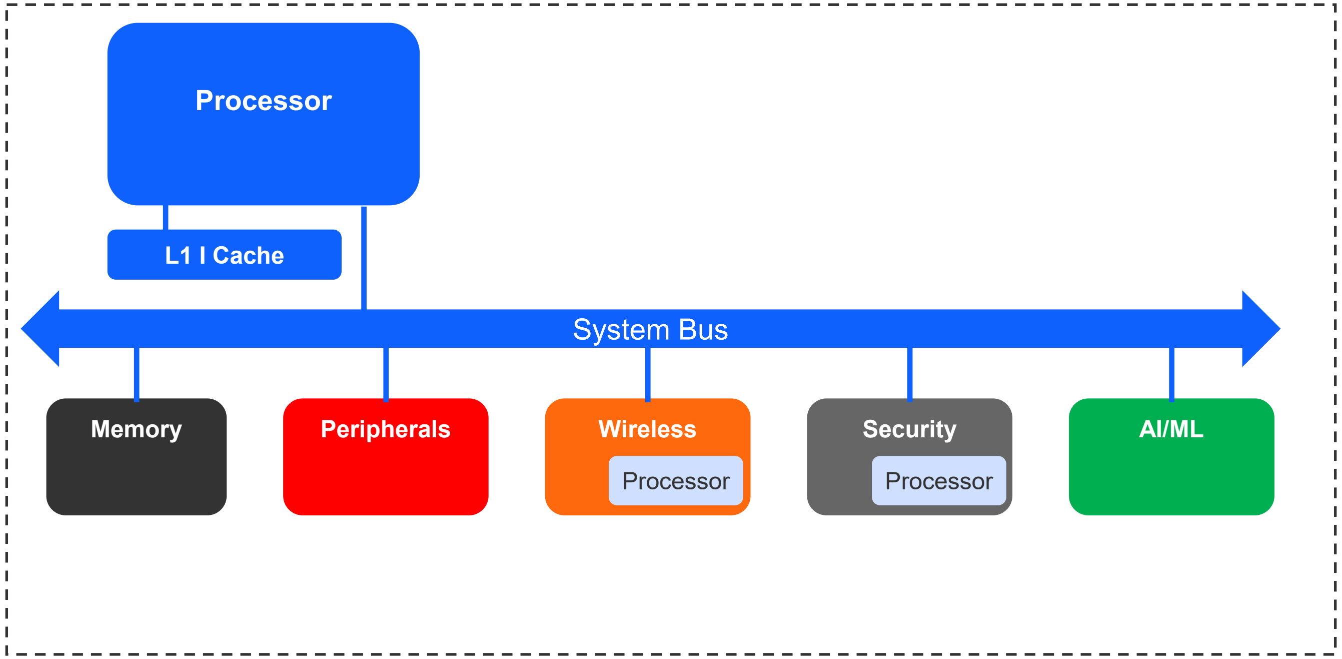
- Application Use Case
  - Acceleration needed to service the requirement (Object classification, Wake word detection, Glass break detection) with constraints.
- Power Consumption
  - Acceleration significantly lowers power consumption
- Latency
  - Accelerated performance vs CPU based performance
- Size of the model
  - Memory available for the model both RAM and Flash perspective

Building the IoT Solution



- **Sub-systems create building blocks for today's scalable MCU architectures**
  - All MCUs have 3 common subsystems:
    - Processor Core
    - Memory
    - Peripherals
- **Additional Sub-systems can be added to increase functionality**
  - Wireless
  - Security
  - AI/ML
  - …
- **Commonality between platforms simplifies developer journey**
  - Allows for reuse between MCU families and end-product designs

Multi-core vs Single Core Systems



Poll

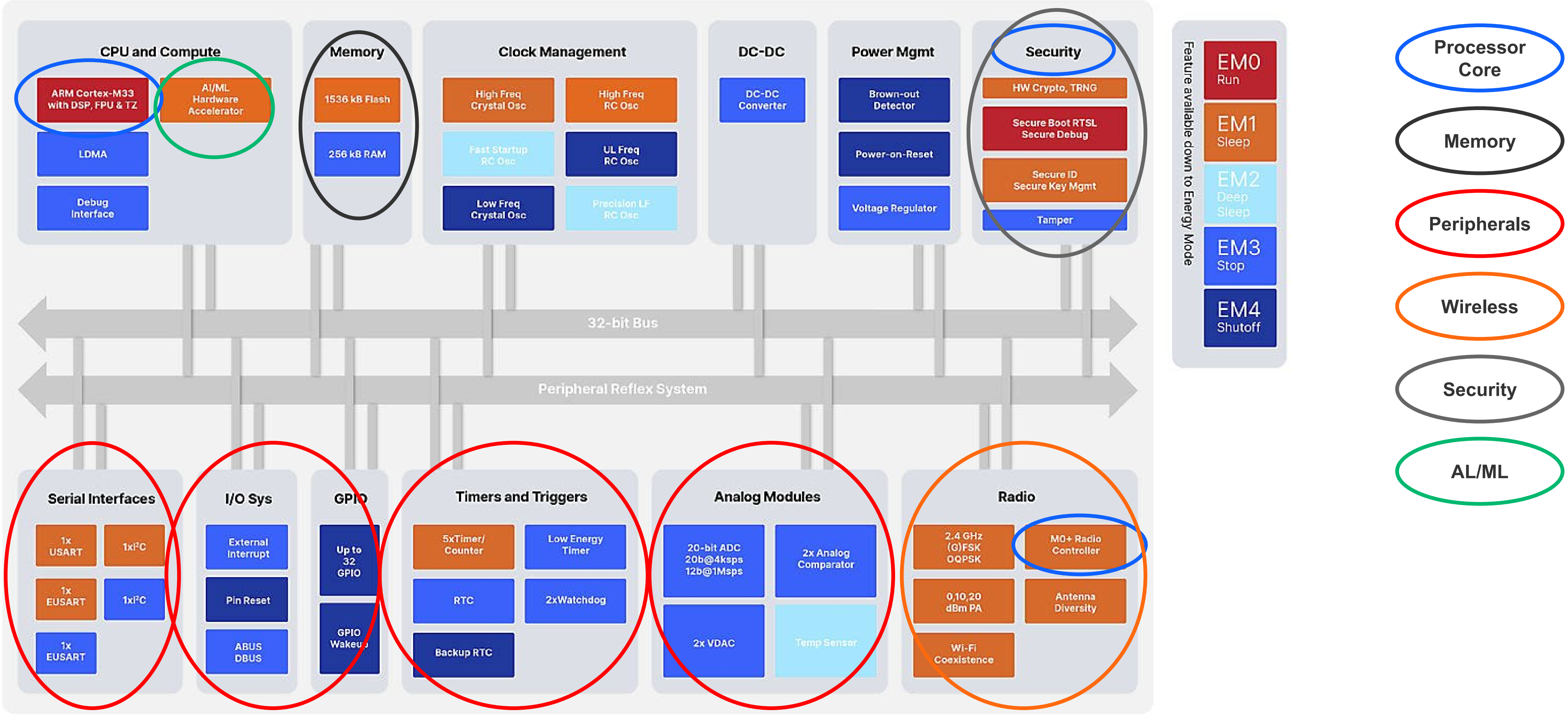
- **User view**: How many cores available for “user” programming?
- **System Architecture View**: How many cores are built into the system?

Key Drivers for Multi Core

- System Efficiency
  - Ex: Radio waking up the rest of the system based on packet detection / sense.
  - Right sizing: Need not keep a larger, higher clocked core for not so intensive activities
- Isolation requirements
  - Security system
  - Meeting radio timings

> *“A rose by any other name would smell as sweet”* - William Shakespeare

xG24 – A product in action



Q&A

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Silicon Labs’ Approach

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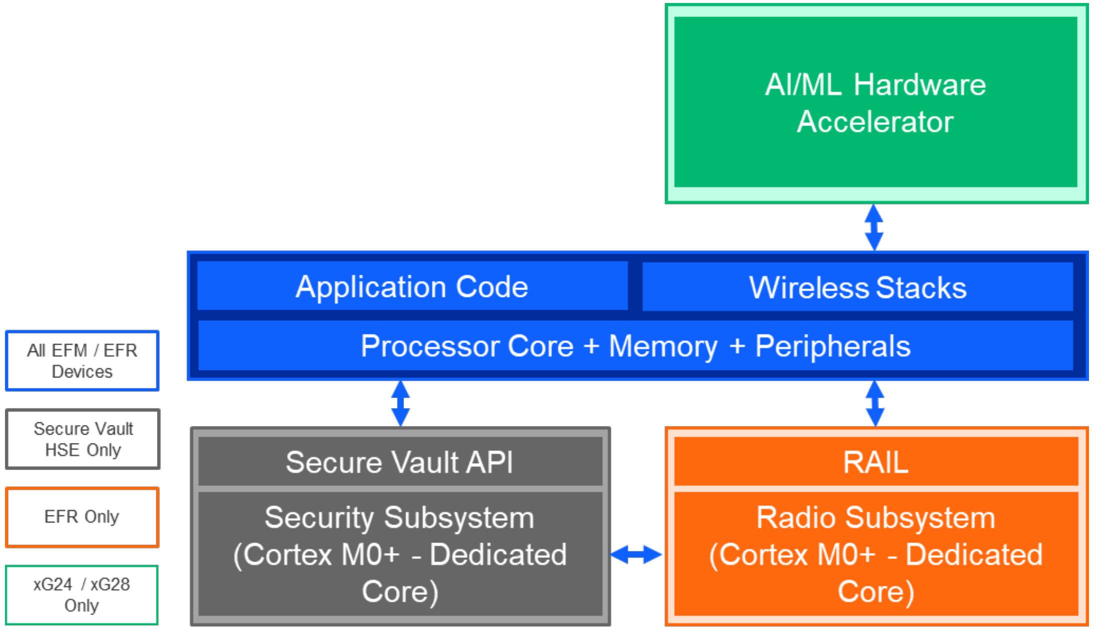
EFM and EFR: Multi-core Solutions for IoT Development


AI/ML Hardware Accelerator
Application Code
Wireless Stacks
Processor Core + Memory + Peripherals
Secure Vault API
Security Subsystem (Cortex M0+ - Dedicated Core)
RAIL
Radio Subsystem (Cortex M0+ - Dedicated Core)
All EFM / EFR Devices
Secure Vault HSE Only
EFR Only
xG24 / xG28 Only

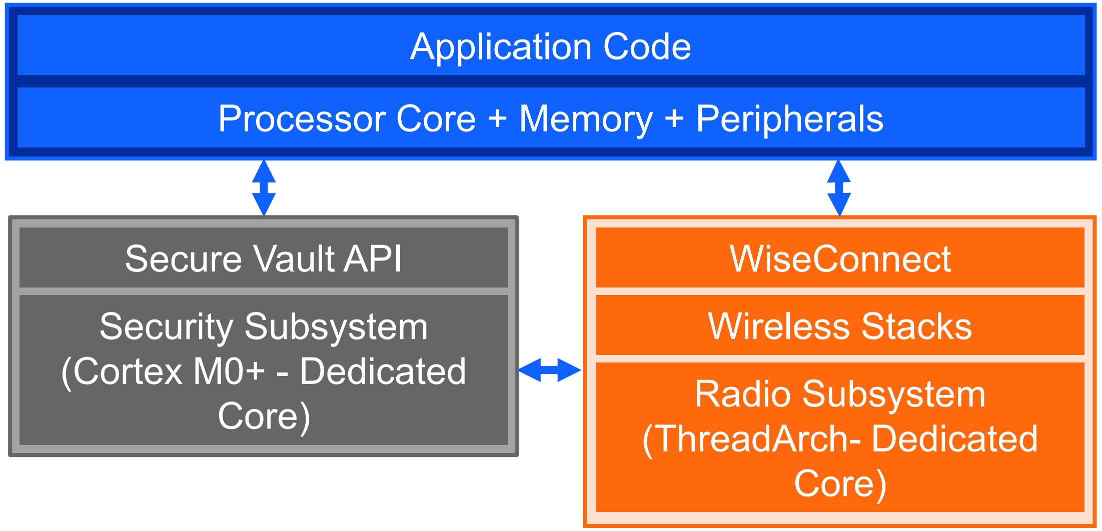
- **Multi-core architecture gives design flexibility and optimization across EFM and EFR platforms**
  - Dedicated application, radio[1], and security[2] cores share system burden for better resource utilization
- **Common Security and AI/ML subsystems**
  - Allows for design consistency independent of connectivity needs
- **Common development platform for connected and non-connected products**
  - Simplicity Studio gives developers a common development platform for entire product portfolio
- **Footprint and firmware compatibility between EFM and EFR families**
  - Simplified SKU management and code base development lowers development cost and complexity

	BG	MG	FG	ZG	SG	PG
xG21	✓	✓				
xG22	✓	✓				✓
xG23			✓	✓	✓	✓
xG24	✓	✓				
xG25			✓			
xG27	✓	✓				
xG28			✓	✓	✓	✓
	EFR Device Families					**EFM**

[1] EFR32 devices only [2] Secure Vault Hardware Secure Element (HSE) Only

Wi-Fi Products – RS9116 and SiWx91x

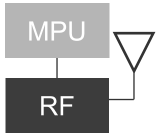
- **Wi-Fi products deviate from EFR / EFM platform architecture**
    - NCP and SoC options depending on application needs
- **NCP focused on wireless operation only**
    - Removes customer accessible application core for ease of use
- **SoC creates true Wi-Fi + Bluetooth LE SoC**
    - Wireless stacks and operation handled entirely by radio subsystem
    - Application core fully available for end product development


Application Code
Processor Core + Memory + Peripherals
Secure Vault API
Security Subsystem (Cortex M0+ - Dedicated Core)
WiseConnect
Wireless Stacks
Radio Subsystem (ThreadArch- Dedicated Core)

Bandwidth and compute are correlated

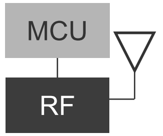
Systems have one of three architectures

Big digital plus wireless co-processor



The application processor (MPU) runs large operating system and customer applications. Wireless chip runs the wireless stack.

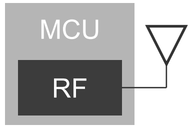
Little digital plus wireless co-processor



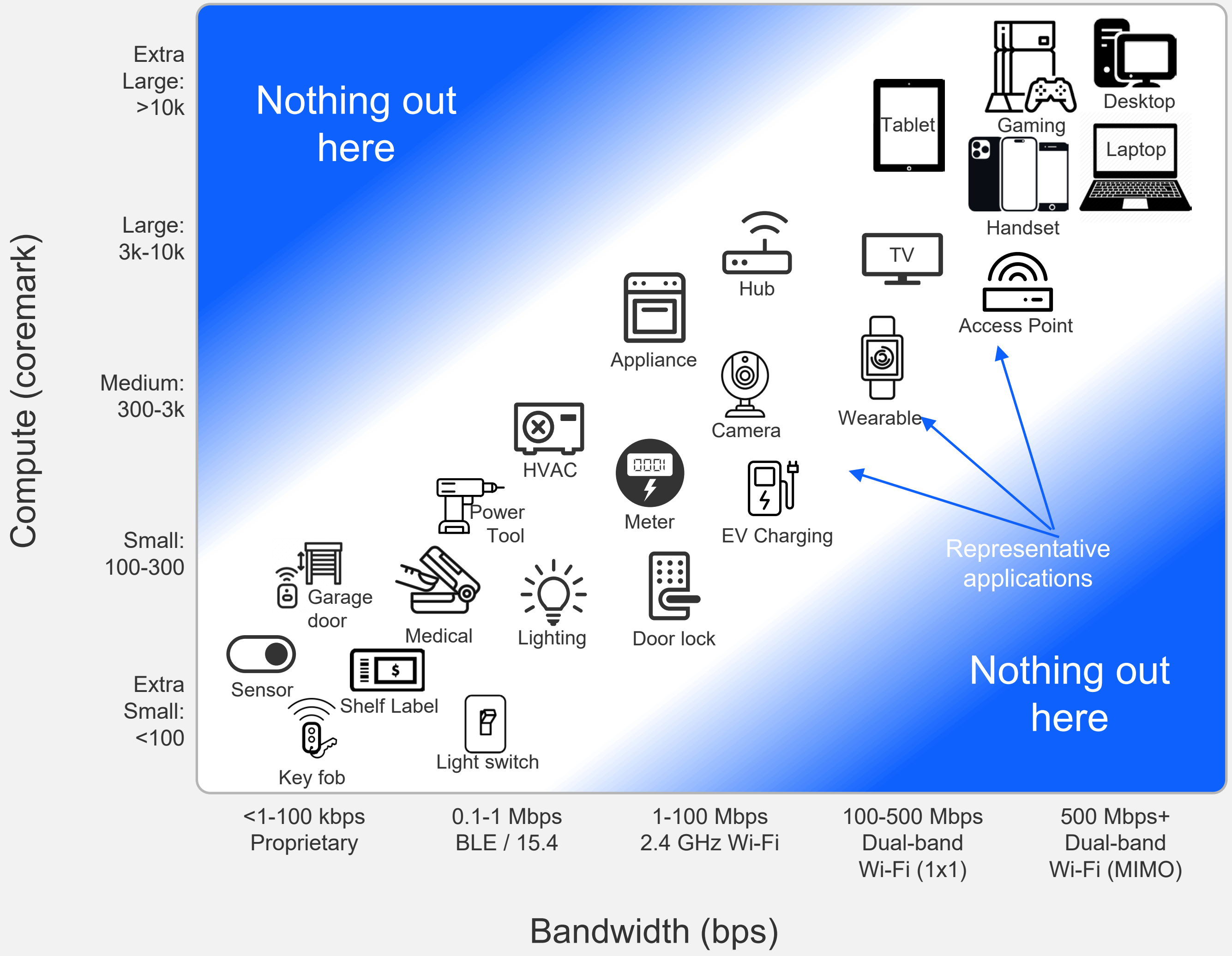
The application processor (MCU) runs bare metal or with light real-time operating system and customer applications. Wireless chip runs the wireless stack.

Key Market Trend: Power, Cost & form factor advantages, reduced complexity

One system SoC



There is only one chip in the system. It runs both the application software and the complete wireless connectivity solution.



Summary

- **Multiple sub-systems come together in an MCU based on the category**
  - Simple MCUs, Secure MCUs, Secure Wireless MCUs, AI+ML enabled Secure wireless MCUs
- **Several considerations at each subsystem level determine the choice of the MCU platform**
  - Application complexity, execution constraints, interfaces to the real world, security considerations, connectivity & AI/ML use cases
- **Silicon Labs has portfolio across all these categories serving both connected and non-connected devices using the same development environment**

Q&A

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Thank You

Watch ON DEMAND

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